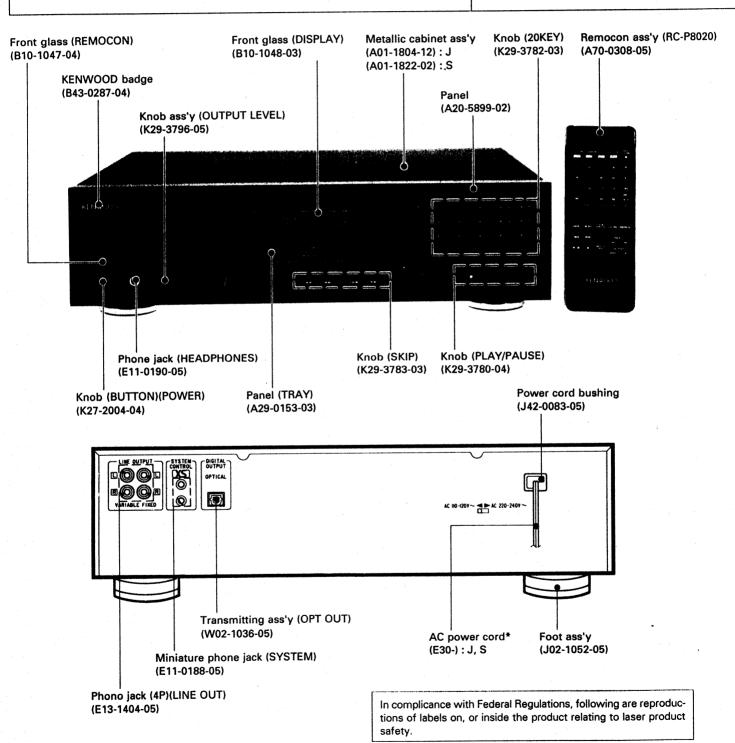
COMPACT DISC PLAYER

DP-7020 SERVICE MANUAL

KENWOOD

© 1989-10 PRINTED IN JAPAN B51-3992-00 (O) 3354



J : Japan made

S: Singapore made

*Refer to parts list on page 73.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.

AVOID DIRECT EXPOSURE TO BEAM.

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| DP-7020 | JAPAN MADE | SINGAPORE MADE |
|-----------------|------------------------|--------------------|
| CONTROL UNIT* | X32-1510-11 (K, P) | X32-1562-71 (T, E) |
| | X32-1510-21 (U, UE, M) | X32-1560-10 (K) |
| | X32-1512-71 (X) | |
| MECHANISM ASS'Y | X92-1370-02 | X92-1400-02 |
| | (CDM-14) | (CDM-14SA) |

Caution:

The mechanism ass'y used with the DP-7020 varies in two types depending on the manufacturing location. (Japan, Singapore)

Before Operation

• Transportation screw

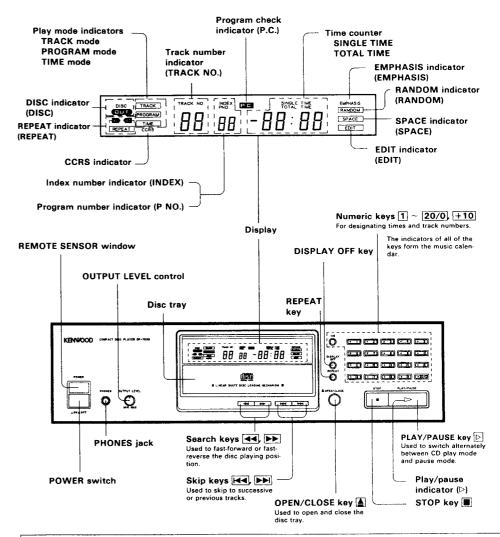
Before operation, remove the red-headed screw attached to the bottom of the unit used during transportation from the factory. Remove the screw using a coin or screwdriver,

- · After removing, retain the screw together with the Warranty card and other documents.
- When the unit is to be transported again, be sure to replace the screw to its original position.
- 1. Turn ON the power switch when no disc is loaded.
- 2. Wait a few seconds until the disc OUT indicator comes "ON". Then turn "OFF" the power.



3. Firmly tighten the transportation screw

CONTROLS AND INDICATORS



DISPLAY OFF key

If the DISPLAY OFF key is pressed during disc play, the display is extinguished.

- If the DISPLAY OFF key is pressed at any time other than during disc play, the display will not be extinquished.
- When an operation key is pressed (excluding adjustment of the OUTPUT LEVEL control) while the display is in the DISPLAY OFF state, the display appears for a few seconds
- When the display is in the DISPLAY OFF state during program play, the display appears for approximately 2 seconds at the beginning of each

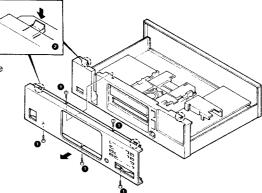
The DISPLAY OFF state is canceled when the DISPLAY OFF key is pressed again or when the OPEN/ CLOSE key a or STOP key is pressed.

DISASSEMBLY FOR REPAIR

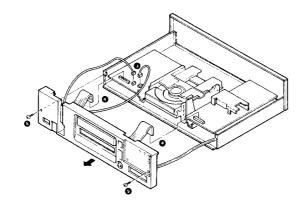
1. How to remove the operation unit and mechanismass'y

1. Remove the 5 screws (1).

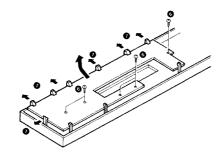
2. Push the projection of the front panel and remove the panel (2).



- 3. Remove 2 connectors (3).4. Pull out the 2 flexible Cables (4).
- 5. Remove the screw (6) and sub panel.

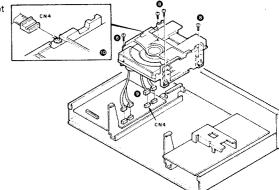


- 6. Remove the 5 screws (6).
- 7. Slide the projections and remove pc board ass'y ().



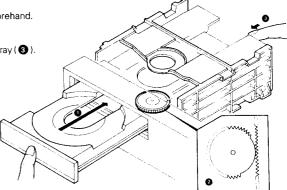
DISASSEMBLY FOR REPAIR

- 8. Remove the 4 screws (3).9. Remove the 4 connectors (3).
- 10. When removing the mechanism ass'y, () first set the short pin.

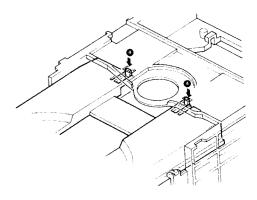


2. Removing the tray

- With the tray open, turn off the power beforehand.
 Push in the tray slowly by a hand ().
- In this situation, the gear is free (2).
- 3. Push the tray towards you and draw out the tray (3).

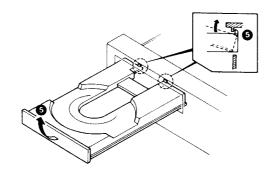


Push down off the two catches () of the tray stopper, and draw out the tray in the direction of an arrow.



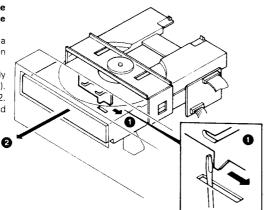
DISASSEMBLY FOR REPAIR

 When removing the tray, detach it in the direction of arrow () in which it can be detached without the sub panel caught by the tray stopper.



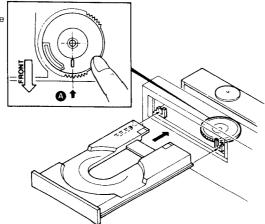
2-1. When the power is not turned on or when the tray does not come out even by pressing the OPEN key

- Push the lever by a screwdriver, etc. put in through a slit on the bottom plate of the product as shown on the right ().
- 2. Thereby, the gear will be free with the tray slightly advanced. Thus, draw out the tray towards you (2). Otherwise, as previously stated in step 3. of "2. Removing the tray", push the tray towards you and draw out the tray.



3. Installing the tray

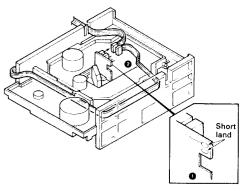
- 1. Set to location ((A)) the protrusion on the upper side of the gear as shown on the right.
- 2. Push in the tray along the left and right guides.



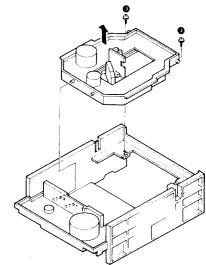
DISASSEMBLY FOR REPAIR

3. Removing the Pickup (Japan made)

- 1. Turn over the mechanism and short the short land of the pickup (1).
- 2. Disconnect the two connectors (2).

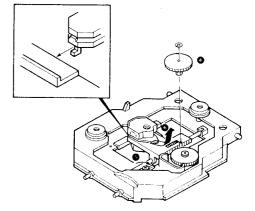


3. Remove the two screws (3), then remove the MD assembly.

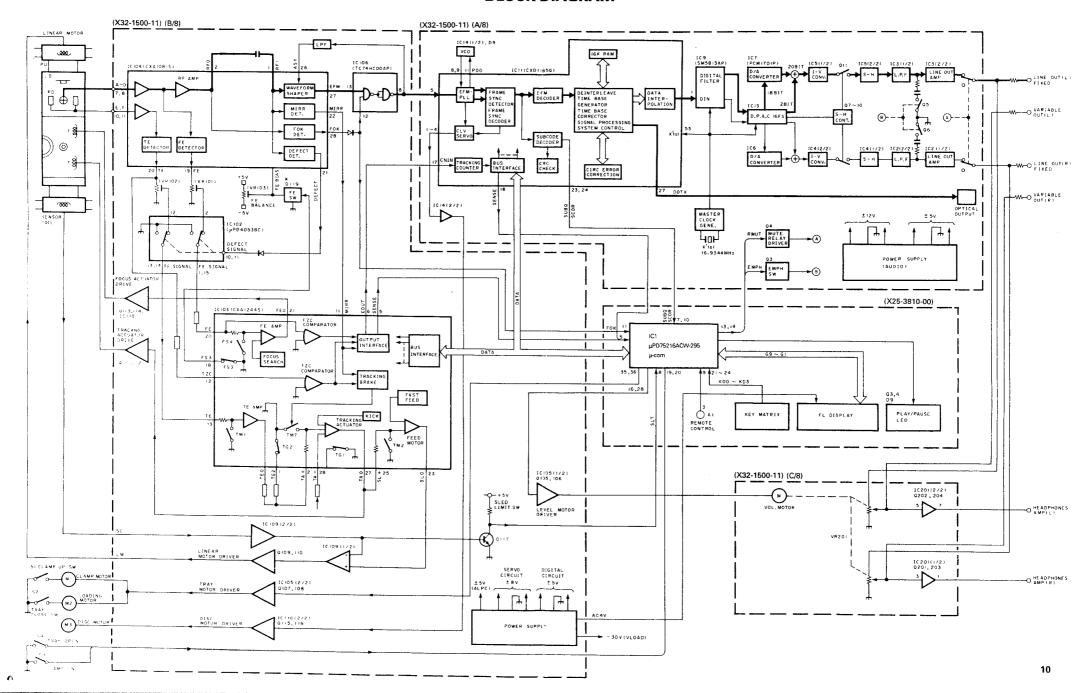


- 4. Remove the snap ring, then remove the gear (4).
- 5. Remove the stopper (5).
- Remove the pickup in the direction of the arrow ().
 Note: When installing the pickup, in the reverse order of disassembly.

Unsolder the short land after connecting the connector.



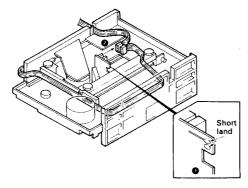
DP-7020 DP-7020 BLOCK DIAGRAM



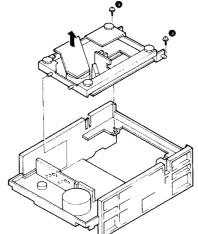
DISASSEMBLY FOR REPAIR

3. Removing the pickup (Singapore)

- Turn over the mechanism and short the short land of the pickup ().
- 2. Disconnect the two connectors (2).

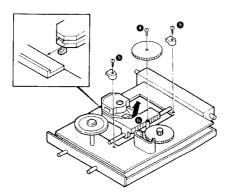


3. Remove the two screws (3), then remove the MD assembly.



 Remove the screw, then remove the gear ().
 Remove the stopper ().
 Remove the pickup in the direction of the arrow ().
 Note: When installing the pickup, in the reverse order of disassembly.

Unsolder the short land after connecting the connector.



CIRCUIT DESCRIPTION

1. Description of components

1-1. CD PLAYER UNIT (X32-1500-11)

| Ref. No. | Part. No. | Use/Function | Operation/Condition/Compatibility | | | | |
|--------------|----------------------|---|---|--|--|--|--|
| IC1 | NJM4565D | Power Supply | For analog circuit of DAC. | | | | |
| IC2, 3 | NJM4565D | L.P.F | 2nd low pass filter and amplifier for output. | | | | |
| IC4, 5 | NJM4580D | I/V Converter | Conversion of D/A converter current output into voltage from. (Refer to | | | | |
| 1 | | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | D.P.A.C at page 15) | | | | |
| IC6, 7 | PCM1701P | DAC | Conversion of 18bit digital data into analog one. | | | | |
| IC8 | NJM4565D | Power supply (+5V) | For oscillation (IC10), Digital filter (IC9) and HIC. | | | | |
| IC9 | SM5813AP | Digital filter | Convert 16bit FS to 20bit 8FS. | | | | |
| IC10 | TC74HCU04AP | Oscillation | Oscillation master clock 16.9344MHz and applied clock signal to IC9,11, | | | | |
| | | | and 13. | | | | |
| IC11 | CXD1165Q | Digital signal processor | All digital signal processing operation, Including the EFM data demodulator, | | | | |
| | | | error correction, interpolation circuit, PLL, CLV, Digital output jitter free. | | | | |
| IC12 | NJM4565D | Power supply (+5v) | For IC11,15 and IC14 of PLL and CLV. | | | | |
| IC13 | KAG01 | Bit converter | Add 2bit to 18bit DAC and 18bit to 20bit jitter free. (refer to circuit descrip | | | | |
| | 101001 | and conventor | tion at page 40) | | | | |
| IC14 | NJM4565D | PLL, CLV servo | Servo amplifier for disk motor and control VCO freq. by phase comparation | | | | |
| | 11011110000 | 1 22, 021 00110 | signal. | | | | |
| IC15 | TC74HC00AP | Data select | No use for repair. | | | | |
| IC101 | NJM4558D | Power supply (+5V) | For servo circuit. | | | | |
| IC102 | μPD4053BC | Defect circuit | If RF signal defect (IC104 Defection), servo circuit is open and playback go | | | | |
| | μ. ο τουσσο | B Groot Girodit | on. | | | | |
| IC103 | CXA1244S | Servo signal processor | Control of focusing error tracking servo and feed servo pulses for servo | | | | |
| .0.00 | 0,0112440 | Corro signar processor | control. | | | | |
| IC104 | CXA1081S | RF amplifier | Focusing error signal generator, tracking error signal generator, RF signal | | | | |
| 10104 | CARTOOTS | ru ampiner | generator and phase componsation. | | | | |
| IC105 | NJM4558D | Motor control | For motor of OPEN/CLOSE and one of UP/DOWN. | | | | |
| IC106 | TC74HC00AP | Buffer amplifier | For EFM signal to signal processor. | | | | |
| IC109 | NJM4558D | Amplifier | For sled drive of pickup travel. | | | | |
| IC110 | NJM4558D | Amplifier | For focus actuator drive and disk motor. | | | | |
| IC201 | NJM4565D | Amplifier | For headphone. | | | | |
| Q1 | 2SB941 | Power supply (+) | For analog circuit. | | | | |
| Q2 | 2SD1266 | Power supply (-) | For analog circuit. | | | | |
| Q3 | DTC124EN | Inter face | For emphasis and micro processor. | | | | |
| Q4 | 2SC1740S | Inter face | | | | | |
| Q5, 6 | 2SC2878 | Switch | For relay, micro processor and relay drive. | | | | |
| Ω7, 8 | 2SA1206 | Inter face | For emphasis. | | | | |
| Q9, 10 | 2SK246 | | For sample-hold circuit and inter face of clock signal. | | | | |
| Q11, 12 | 2SK152 | Power supply Switch | When Q7, 8 are off condition, Q11, 12 are off. | | | | |
| Q13, 14 | 2SC3940A | Power supply (+5) | Control the gate Q7~10. If on, sample mode. If off, hold mode. For DAC. | | | | |
| Q15, 14 | 2SC3940A | Power supply (+5) | For digital filter (IC9). | | | | |
| Q16 | 2SC3940A | Power supply (+5V) | For oscillation (IC10). | | | | |
| Q17 | 2SA1534A | Power supply (-5V) | For PLL and CLV. | | | | |
| Q18 | 2SC3940A | Power supply (+5V) | | | | | |
| Q19 | 2SK246 | Power supply (+5V) | For PLL, CLV and signal processor. | | | | |
| Q20 | 2SA933S | Muting amplifier | Control output of nation) when now P. # PF. (| | | | |
| Q21 | 2SC733 (A) | widing ampliner | Control output of optical when power on. Buffer amplifier for optical output | | | | |
| Q101 | 2SA1534A | Power oun-by (- 5) | For apply circuit | | | | |
| Q102 | 2SC3940A | Power supply (+5) | For servo circuit. | | | | |
| | | Power supply (-5V) | For servo circuit. | | | | |
| Q103 | 2SD1944 | Power supply (+5V) | For FL-indicator. | | | | |
| Q104 Q105 | 2SA1534A 2SA1534A | Power supply (-30V) | For FL-indicator. | | | | |
| Q106 | | Buffer | Drive motor of VOLUME. | | | | |
| | 2SC3940A 2SA1534A | Buffer | Drive motor of tray. | | | | |
| Q107 | | | | | | | |

SINGAPORE MADE

DP-7020

CIRCUIT DESCRIPTION

| Ref. No. | Part. No. | Use/Function | Operation/Condition/Compatibility |
|----------|-------------------|--------------|---|
| Q109 | 2SA1534A | Buffer | Drive feed motor. |
| Q110 | 2SC3940A | | |
| Q111 | 2SA1534A | Buffer | Drive actuator of tracking. |
| Q112 | 2SC3940A | | |
| Q113 | 2SA1534A | Buffer | Drive actuator of focusing. |
| Q114 | 2SC3940A | | |
| Q115 | 2SA1534A | Buffer | Drive disk motor. |
| Q116 | 2SC3940A | | |
| Q118 | 2SA11534A | Buffer | For laser diode and ALPC. |
| Q119 | 2SC1740S (Q, R) | Switch | When focus servo is on FE BIAS circuit works. |
| | 2SC945 (A) (Q, R) | | |
| Q201 | 2SC3666 | Buffer | For head phone. |
| Q202 | | | |
| Q203 | 2SA1426 | | |
| Q204 | | | |

1-2. DISPLAY AND µ-COM UNIT (X25-3810-00)

| Ref. No. | Part. No. | Use/Function | Operation/Condition/Compatibility |
|----------|--------------------------------------|----------------|--|
| IC1~3 | TD62801P | Inverter | Convert data (Serial parallel), For 20KEY LED. |
| IC4 | µPD75216ACW-295 | Microprocessor | - |
| IC5 | M51951ASL | Reset IC | For reset of microprocessor. |
| Q1, 5 | 2SC1740S (Q, R) 2SC945 (A) (Q, R) | Buffer | For FL-indicator of pin1 and pin9. |
| Q2 | DTA124EN | Buffer | For VOLUME LED. |
| Q3, 4 | DTA124EN | Power supply | For reset IC. |

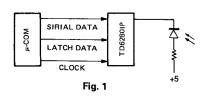
2. Display unit u-com unit

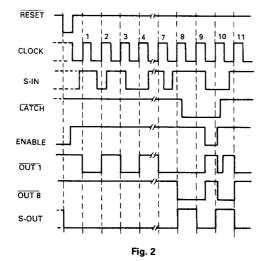
•Turning on the self-illuminating 20KEY LED's

The self-illuminating 20KEY LED's are turned on with the 8-bit shift register (TD62801P). The microprocessor sends the serial data, latch data, and clock to turn on the 20KEY, PLAY, and PAUSE LED's.

Three units of TD62801P are used and connected respectively by S-OUT and S-IN. The data are output by setting the enable terminal to "H" level.

Fig.1 shows the rough block diagram for turning on the LED's and Fig.2 shows the timing chart.





CIRCUIT DESCRIPTION

· D.P.A.C (Digital Pulse Axis Control) circuit

Two different distortions are attendant on the conversion of the digital signal into an analog signal. One is a distortion on the level axis (voltage axis), which is determined mainly by the resolution of the D/A converter, and in case of using a ladder resistor type, by its error.

The other is a distortion on the time axis, which is not so prevailing as to appear on the distortion meter but has great influence on the sound quality. It is the D.P.A.C that is to operate as a circuit to improve this point.

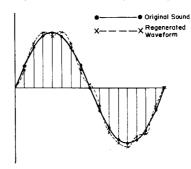


Fig. 3 Error (distortion) on voltage axis

Figure 2-3 shows the error (distortion) on the voltage axis of the D/A converter output for the original sound, and Figure 2-4 shows the error (distortion) on the time axis of the D/A converter output for the original sound.

As seen from this, even with a variation in time axis, there appears a regenerated waveform different from the original sound.

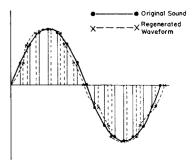
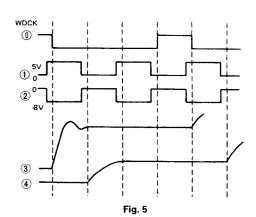


Fig. 4 Error (distortion) on time axis

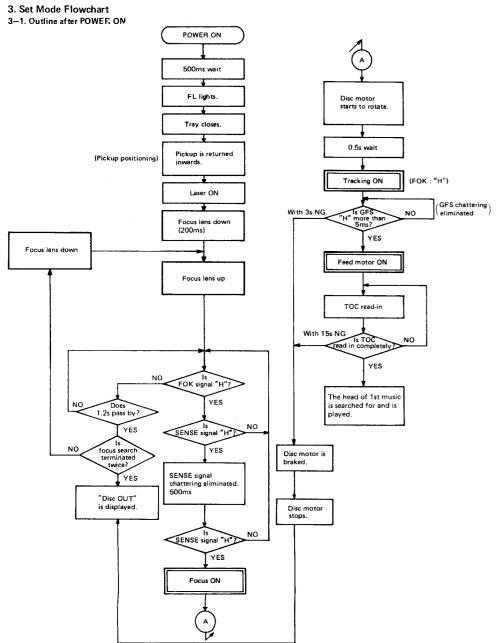
. D.P.A.C by sample holding (S-H) circuit

The model of this time has the D.P.A.C circuit on the basis of an S-H circuit which has been more improved than the conventional D.P.A.C.

This new S-H circuit has the same composition as the conventional one. The difference between them is that the former uses the clock obtained by dividing the master clock for the sample holding signal which does not have jitters. This clock is converted into an analog signal, than its time axis corrected (its jitters are eliminated). The D/A conversion is carried out at 8 FS, but the sample holding clock is set to 16 FS. Accordingly, the noises generated in the S-H circuit is raised to 16 FS, thus the effects on the audio signal is minimized.



CIRCUIT DESCRIPTION



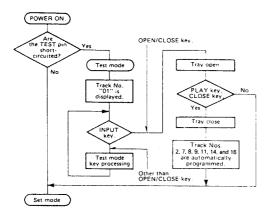
DP-7020

CIRCUIT DESCRIPTION

4. Test mode

With the DP-7020, the microprocessor can be set to test mode by short-circuiting pin 7 and pin 8 of the CD PLAYER UNIT (X32-1500).

Note: "Set mode" shows the normal status.

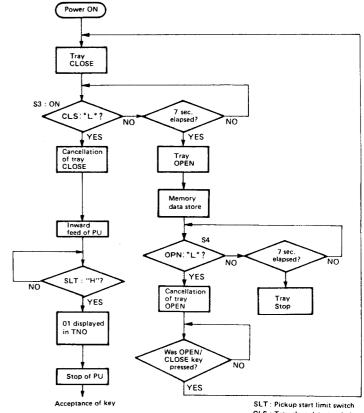


4-1. Key and functions valid in test mode

| No. | Input key | Function | Track No. display |
|-----|-------------|---|--|
| 1 | PLAY | (1) Focusing servo ON (2) Tracking servo ON (3) Feed servo ON | PLAY (b) Key lights |
| 2 | STOP | Jump to the first stop of TEST mode. | Disk track No.and time are displayed |
| 3 | UP 🕪 | (1) Focusing servo ON (2) Tracking servo OFF (3) Feed servo OFF | TRACK NO T - 1 PAUSE (11) blinking P.C lights. |
| 4 | DOWN 🖊 | (1) Tray Opened (2) Laser ON The TEST mode goes on when the tray is closed by pressing the tray. | TRACK NO. 1 2 REPEAT lights |
| 5 | FF ▶ | In the STOP mode, moves the pickup slightly toward the outer position of disc. | Name of the Control o |
| 6 | FB ≪ | In the STOP mode, moves the pickup slightly toward the inner position of disc. | |
| 7 | OPEN/CLOSE | When the tray is opened and the closed again in test mode, Track Nos 2,7,8, 9,11,14, and 16 are automatically programmed. | |
| 8 | DISPLAY OFF | All of FL's segments are light and PLAY and PAUSE indicator light. | |

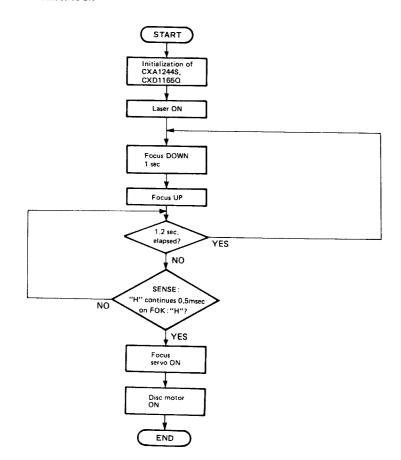
CIRCUIT DESCRIPTION

- 4-2. Flow chart of test mode
- Flow chart from tray OPEN status after power ON



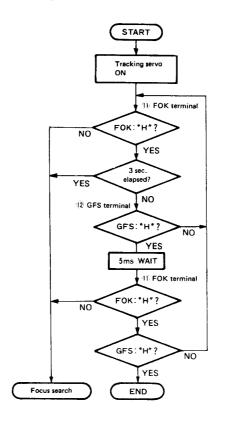
CIRCUIT DESCRIPTION

Focus search & focus servo ON

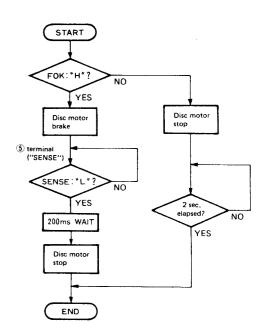


CIRCUIT DESCRIPTION

Tracking servo ON



Disc motor STOP

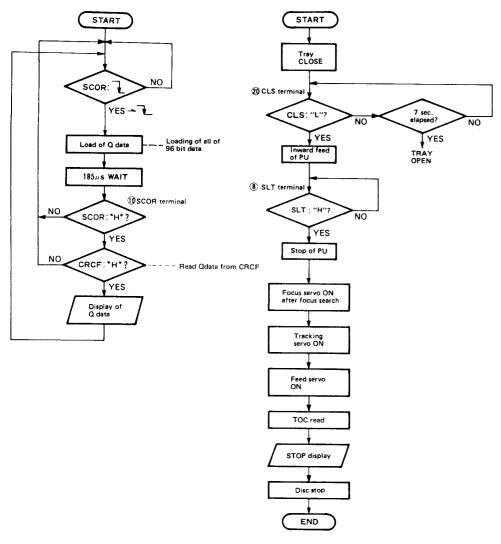


DP-7020

CIRCUIT DESCRIPTION

• From loading of Q data to display

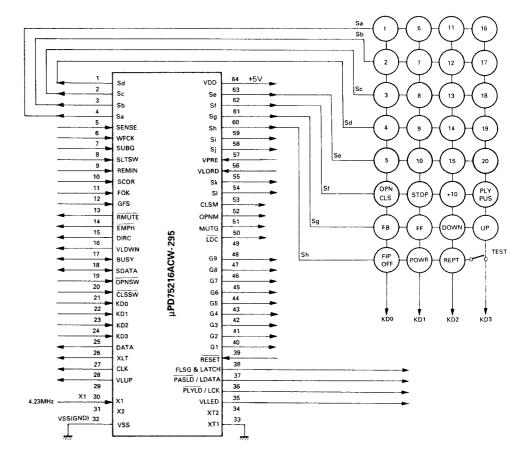
 In a usual case, since the tray was pushed when the tray is OPEN until STOP display is made.



CIRCUIT DESCRIPTION

 $\textbf{5.Microprocessor}~\mu\textbf{PD75216ACW-295}~(\textbf{X25-3820-00}:\textbf{IC1})$

5-1. Terminal connection diagram



CIRCUIT DESCRIPTION

5-2. Explanation of terminals

| Pin No. | Pin Name | i/0 | Function |
|---------|----------|----------------|--|
| 1~4 | Pd~Pa | 0 | FL segment control pins (also for key signal). |
| 5 | SENSE | 1 | Signal processing, pin to detect the SENSE signal from servo IC. |
| 6 | WFCK | 1 | Q data read-out clock pulse input pin. |
| 7 | SUBQ | 1 | Q data input pin. |
| 8 | SLTSW | 1 | Pickup stops (STOP: "H"). |
| 9 | RCI | ı | Remoto control input pin. |
| 10 | SCOR | 1 | Sub-code frame sync detection signal input pin. |
| 11 | FOK | 1 | RF amplifier FOK signal input pin (At focus OK : "H"). |
| 12 | GFS | 1 | Frame sync signal input pin (In frame sync : "H"). |
| 13 | REMUTE | 0 | Relay mutes (ON: "L"). |
| 14 | EMPH | 0 | De-emphasis control pin (ON : "L"). |
| 15 | DIRC | 0 | Servo IC DIRC pin . |
| 16 | VLDWN | 0 | Volume control level goes down. |
| 17 | BUSY | 1/0 | BUSY signal of serial data. (System control) |
| 18 | SDATA | 1/0 | Data signal of serial data. (System control) |
| 19 | OPNSW | I | Tray open switch (When open : 'L"). |
| 20 | CLSSW | 1 | Tray close switch (When close : 'L'). |
| 21~24 | KD0~KD3 | 1 | Key matrix key return input pins. |
| 25 | DATA | 0 | Signal processing, servo IC control output pin (Control data signall). |
| 26 | XLT | 0 | Signal processing, servo IC control output pin (Control data latch signal). |
| 27 | CLK | 0 | Signal processing, servo IC control output pin (Control data transmission clock signal). |
| 28 | VLUP | 0 | Volume control level goes up. |
| 29 | - | | Unused. |
| 30 | X1 |) | System clock pulse input pin. |
| 31 | - | | Unused. |
| 32 | Vss | _ | GND. |
| 33 | XTI | - | GND. |
| 34 | - | | Unused. |
| 35 | VLLED | 0 | LED for positioning output level (Blink : LEVEL varia). |
| 36 | PLYLD | 0 | PLAY LED lights. |
| 37 | PASLD | 0 | PAUSE LED lights. |
| 38 | FLSG | 0 | Key scan signal when FL OFF (FL OFF : "H"). |
| 39 | RÉSET | ī | Reset input pin (Active 'L'). |
| 40~48 | G1~G12 | 0 | FL digit control pins. |
| 49 | N.C | _ | Unused. |
| 50 | LCD | 0 | Signal for laser ON/OFF (Active "L"). |
| 51 | MUTG | 0 | Muting signal for signal processor. |
| 52 | OPNM | 0 | Tray OPEN/CLOSE signal (Active "H"). |
| 53 | CLSM | 1 | The state of the s |
| 54,55 | SI,Sk | 0 | FL segment control pins (also for key scan signal). |
| 56 | VLOAD | 1 | FL driver negative power supply (~30V). |
| 57 | VREF | Ħ | FL pre-driver negative power supply (~50V). |
| 58~63 | Pi~Pe | 0 | FL segment control pins (also for key scan signal). |
| 64 | VDD | _ | Power supply (+5V). |
| | | | |

CIRCUIT DESCRIPTION

6. RF AMP CXA1081S (X32-1500-11: IC104)

General

The CXA1081S is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- · A minimum of external parts required.
- · A disc defect detector circuit for improved playability.

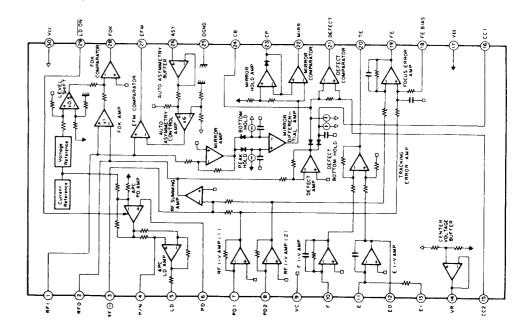
Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- . Focus OK detector circuit
- · Mirror detector circuit
- · Tracking error amplifier
- · Defect detector circuit
- APC circuit
- EFM comparator
- · Auto asymmetry control amplifier

6-1. Block diagram



CIRCUIT DESCRIPTION

6-2. Explanation of terminals (V_{CC}=2.5V, V_{EE}=D_{GND}=-2.5V, VC=GND)

| Terminal No. | Terminal I/O | | DC voltage (V) | Function | | | |
|-----------------|--------------|-----|-------------------|--|--|--|--|
| 1 | RFI | 1 | 0 | Input pin for the C-coupled signal output from the RF summing amplifier | | | |
| 2 | RFO | 0 | Vern | RF summing amplifier output pin. Used as the check point for the eye pattern | | | |
| 3 | RF⊖ | - 1 | 0 | RF summing amplifier feedback input pin | | | |
| 4 | PrN | . 1 | 0 (VC) | P-sub/N-sub select pin for the LD (Laser Diode) (DC voltage: in N-sub mode) | | | |
| 5 | L.D | 0 | - 1.8 | *APC LD amplifier output pin_(DC voltage: PD open in N-sub mode) | | | |
| 6 | PD | - 1 | . 0 | *APC LD amplifier input pin_(DC voltage_open) | | | |
| 7 | PD1 | . 1 | 0 | RF I-V amplifier (1) inverted input pin Current input by connecting to the photodiode A + C terminal | | | |
| 8 | PD2 | 1 | 0 | RFI-V amplifier (2) inverted input pin Current input by connecting to the photodiode B+D terminal | | | |
| 9 | VC | - | 0 | Connected to GND when using a positive (+)/negative (+) dual-voltage power supply Connected to VR (pin 14) when using a single-voltage power supply | | | |
| 10 | ç | 1 | 0 | F.E.V. amplifier inverted input pin Current input by connecting to the photodiode F terminal | | | |
| 11 | E | 1 | 0 | ETV amplifer inverted input pin Current input by connecting to the photodiode Elterminal | | | |
| 12 | EO | 0 | 0 | F I-V amplifier output pin | | | |
| 13 | ΕI | 1 | 0 | f I-V amplifier feedback input pin for E I-V amplifier gain adjustment | | | |
| 14 | VR | 0 | V: 511 | DC voltage output pin of (Vcc + Vtt)/2 | | | |
| 15 | CC2 | 1 | 1.0 | Input pin for the C-coupled signal output from the defect bottom hold | | | |
| 16 | CC1 | 0 | 1.2 | efect bottom hold autput pin | | | |
| 17 | Viii | | - 2.5 | Connected to the negative power supply when using a positive (+) negative (+) dual-voltag power supply. Connected to GND when using a single-voltage power supply. | | | |
| 18 | FE BIAS | 1 | 0 | Bias pin on the focus error amplifier non-inverted side For CMR adjustment of the focus error amplifier | | | |
| 19 | εE | 0 | Ves | Focus error amplifier output pin | | | |
| 20 | TE | 0 | Viii | Fracking error amplifier output pin | | | |
| 21 | DEFECT | 0 | Vpi,rt | Defect comparator output pin (DC voltage, connected to a 10 k-ohm load) | | | |
| 22 | MIRR | 0 | Vaur | Mirror comparator output pin IDC voltage connected to a 10 k-ohm load) | | | |
| 23 | CP | 1 | - 1.3 | Mirror hold capacitor output pin Mirror comparator non-inverted input | | | |
| 24 | СВ | 1 | 0 | Defect bottom hold capacitor connect pin | | | |
| 25 | DGND | | - 2.5 | Connected to GND when using a positive (+) Integrative (+) dual-voltage power supply Connected to GND ($V\epsilon t$) when using a single-voltage power supply | | | |
| 26 | ASY | 1 | - | Auto asymmetry control input pin | | | |
| 27 | EFM | 0 | Virme | EFM comparator output pin. (DC voltage: connected to a 10 k-ohm load) | | | |
| 28 | FOK | 0 | Vios | FOK comparator output pin_(DC voltage: connected to a 10 k-ohm load) | | | |
| 29 | LD ON | ī | - 2.5 (DGND) | LD ON/OFF select pin. (DC voltage: when LD ON) | | | |
| 30 | Vcc | - | 2.5 | Positive power supply. | | | |

^{*}APC Automatic Power Control

CIRCUIT DESCRIPTION

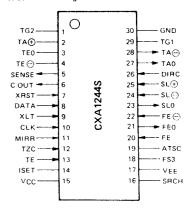
7. Servo control CXA1244S (X32-1500-11: IC103)

CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

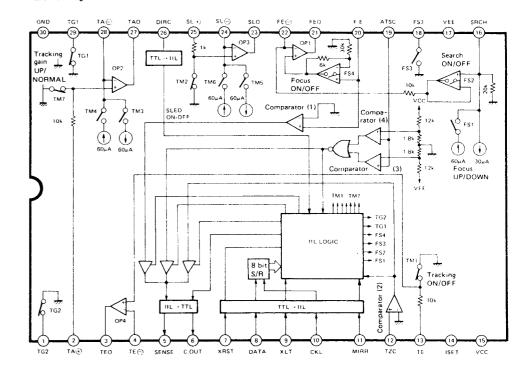
- OFocus control (search ON/OFF, gain control)
- OTracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CXD1125Q.

7-1. Terminal connection diagram



7-2. Block diagram



CIRCUIT DESCRIPTION

| Terminal No. | Terminal name | 1/0 | Functions | | | | |
|--------------|---------------|-----|--|--|--|--|--|
| 1 | TG2 | | Tracking amplifier gain switching terminal, GND level, | | | | |
| 2 | TA ⊕ | | Non-inverted input of operational amplifier 2. | | | | |
| 3 | TEO | | Output of operational amplifier 4. | | | | |
| 4 | TE 🕘 | 0 | Inverted input of operational amplifier 4. | | | | |
| 5 | SENSE | 0 | Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1. | | | | |
| 6 | C. OUT | 0 | Signal output for counting number of tracks at the time of high speed access. | | | | |
| 7 | XRST | Ī | All internal registers are cleared when CPU — SSP "L". Connected with CPU RESET. See Note 2. | | | | |
| 8 | DATA | 1 | Serial data transmission of CPU → SSP, Input is made from LSB, D0~D7. | | | | |
| 9 | XLT | 1 | Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced. | | | | |
| 10 | CLK | 1 | CPU → SSP serial data transmission clock, Data is read at falling. "H" level before and after transmission. | | | | |
| 11 | MIRR | 1 | Mirror signal input from RF amplifier. | | | | |
| 12 | TZC | 1 | Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz. | | | | |
| 13 | TE | 1 | Tracking error signal input, | | | | |
| 14 | ISET | | Setting of current level for determining focus search voltage, | | | | |
| 15 | Vcc | ┼ | tracking jump voltage and sled feed voltage. | | | | |
| 16 | SRCH | | Power supply terminal, Normally –5V. The capacitor for determining the time constant of charge/discharge waveform for focus search is connected. | | | | |
| 17 | VEE | 1 | Power supply terminal. Normally –5V. | | | | |
| 18 | FS3 | + | Focus amplifier gain switching terminal, GND level, | | | | |
| 19 | ATSC | | Such information that a mechanical shock was applied to the player is input. Simply, a trakeing error is input through B.P.F. | | | | |
| 20 | FE | 1 | Input of focus error signal. | | | | |
| 21 | FEO | 0 | Output of operational amplifier 1. | | | | |
| 22 | FE (-) | ti | Inverted input of operational amplifier 1, | | | | |
| 23 | SLO | 0 | Output of operational output 3, | | | | |
| 24 | SL (=) | T | Inverted input of operational amplifier 3. | | | | |
| 25 | SL (+) | T | Non-inverted input of operational amplifier 3. | | | | |
| 26 | DIRC | 1 | Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H" "L" for a fixed length of time with detection of activation, deactivation of TZC. | | | | |
| 27 | TAO | 0 | Output of operational amplifier 2. | | | | |
| 28 | TA (-) | 0 | Inverted input of operational amplifier 2. | | | | |
| 29 | TG1 | 1 | Tracking amplifier gain switching terminal, GND level. | | | | |
| 30 | GND | Т | GND terminal of IC. | | | | |

Note 1 : SENSE terminal output

| Serial data upper 4 bits | ADDRESS | SENSE terminal output | Explanation |
|-----------------------------|---------------------|--------------------------|---|
| 9000 | FOCUS CONTROL | FZC | THE when focus zero cross. Fucus erro vol. signic UV or higher Used at the time of COCUS PUEL opera- tion. |
| 0001 | TRACKING CONTROL | AS | "Hi" when the ATSC input level exceeds the wind comparator level (VTH + + Vcc × 13%). But this is not used in this equipment. |
| 0010 | TRACKING MGDE | 1.2C | Judgement output of positive or negative of tracking error tracking error when used at the time of single tracking error. DIRC is reduced to TU on niteration of TZC for its FWO JUMP or on detection of TZC at REV JUMP. |

Note 2 : Digital unit timing chart Data is loaded at activation

CIRCUIT DESCRIPTION

7-4. System control

| COMMAND | ADDRESS | | | 3 | DATA | | | | SENSE | |
|-------------------|---------|----|----|------------|-------------------|-------|--------|--------|-------|--|
| COMMAND | D7 | D6 | D5 | D4 | D3 | D2 | Dt | D0 | SENSE | |
| | 1 | | | | FS4 | FS3 | F\$2 | FS1 | | |
| FOCUS CONTROL | 0 | 0 | 0 | 0 | FOCUS | GAIN | SEARCH | SEARCH | FZC | |
| | 1 | | | ł | ON | DOWN | ON | UP | 1 | |
| TO ACKING CONTROL | 1 | | n | Ι, | ANTI | BREAK | TG2 | TG1* | 4.0 | |
| TRACKING CONTROL | 0 | 0 | ١٠ | ļ ' | SHOCK | ON | GAIN | SET | AS | |
| TRACKING MODE | 0 | 0 | 1 | 0 | TRACKING* MODE | | SLI | ED* | TZC | |

GAIN SET* TG1, TG2 may be set independently. In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

SLED MODE *

| | D1 | D0 |
|----------|----|----|
| OFF | 0 | 0 |
| SERVO ON | 0 | 1 |
| FWD MOVE | 1 | 0 |
| REV MOVE | 1 | 1 |

TRACKING MODE *

| | D3 | D2 |
|----------|----|----|
| OFF | 0 | 0 |
| SERVO ON | 0 | 1 |
| FWD JUMP | 1 | 0 |
| REV JUMP | 1 | 1 |

DP-7020 DP-7020

CIRCUIT DESCRIPTION

8. Digital signal processor CDX1165Q (X32-1500-11: IC11)

The CXD1165Q is a digital signal processing LSI for a Compact Disc player, and has the following functions.

- 1. Bit clock reproduction by an EFM-PLL circuit
- 2. EFM data demodulation
- 3. Frame sync signal detection, protection and insertion
- 4. Powerful error detection and correction
- 5 Interpolation with an average value, or by holding the previous value
- 6. Demodulation of a sub-code signal, error detection of a sub code Q
- 7. Spindle motor CLV servo

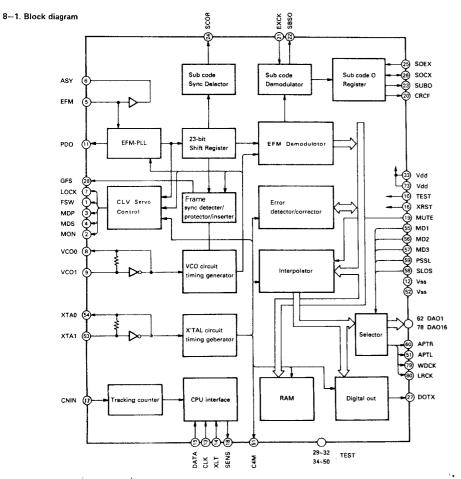
8. 8-bit tracking counter

- 9. CPU interface with a serial bus
- 10. Sub code Q register
- 11. Digital audio interface output
- 12 RAM the entrails.

- · All digital signals used in playback can be processed using only a single chip.
- . An aperture-correction digital filter is built in

Structure

CMOS IC



CIRCUIT DESCRIPTION

8-2. Explanation of terminals

| Terminal No. | Terminal name | 1/0 | Function |
|-----------------|---------------|-----|---|
| 1 | FSW | 0 | Time constant switching output of output filter of spiridle motor |
| 2 | MON | 0 | ON/OFF control output of spindle motor |
| 3 | MDP | 0 | Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode. |
| 4 | MDS | 0 | Drive output of spindle motor. Speed control in CLV-P mode. |
| 5 | EFM | ı | EFM signal input from RF amplifier |
| 6 | ASY | 0 | Output for controlling the slice level of EFM signal |
| 7 | LOCK | 0 | Samples the GFS signal with WFCK/16, and outputs "H" when the level is high When it is "L" for eight times, in arrow, outputs "L" |
| 8 | vcoo | 0 | VCO output f = 8.6436 MHz when locked to EFM signal |
| 9 | VCOI | ı | VCO input |
| 10 | TEST | ı | (0 V) |
| 11 | PDO | 0 | Phase comparison output of EFM signal and VCO/2 |
| 12 | Vss | - | GND (0 V) |
| 13 | CLK | ı | Serial data transmission clock input from CPU. Data is latched at rising edge of a clock |
| 14 | XLT | | Latch input from CPU. Data (senal data from CPU) from the 8-bit shift register is latched in each register. |
| 15 | DATA | 1 | Serial data input from CPU |
| 16 | XRST | 1 | System reset input. Reset at "L" |
| 17 | CNIN | 1 | Input of tracking pulse |
| 18 | SENS | 0 | Output of internal status in correspondence to the address |
| 19 | MUTG | ı | Muting input. In the case when ATTM of internal register A is "1". Normal status when MUTG is "L" or soundless state when it is "H". |
| 20 | CRCF | 0 | Output of result of CRC check of sub code Q |
| 21 | EXCK | ī | Clock input for sub-code serial output |
| 22 | SBSO | 0 | Sub code serial output |
| 23 | SUBQ | 0 | Sub code Q output |
| 24 | SCOR | 0 | Sub code sync S0 + S1 output |
| 25 | SOCK | 1/0 | Sub code O read-off clock |
| 26 | SQEX | 1 | SOCK select input. |
| 27 | DOTX | 0 | DIGITAL OUT output: (Outputs the WFCK signal when CXD11300 or D0 is off) |
| 28 | GFS | 0 | Display output of frame sync lock status |
| 29 | DB08 | 1/0 | H or L position, Don't open circuit. |
| 30 | DB07 | 1/0 | H or L position. Don't open circuit. |
| 31 | DB06 | 1/0 | H or L position. Don't open circuit. |
| 32 | DB05 | 1/0 | H or L position. Don't open circuit. |
| 33 | Voo | Ī - | Power supply (+5 V) |
| 34 | DB04 | 1/0 | H or L position. Don't open circuit. |
| 35 | DB03 | 1/0 | H or L position. Don't open circuit. |
| 36 | DB02 | 1/0 | H or L position, Don't open circuit. |
| 37 | DB01 | 1/0 | H or L position, Don't open circuit. |
| 38 | RA01 | 0 | H or L position. Don't open circuit. |
| 39 | RA02 | 0 | H or L position . Don't open circuit. |
| 40 | RA03 | 0 | H or L position. Don't open circuit. |
| 41 | RA04 | 0 | H or L position. Don't open circuit. |
| 42 | RA05 | 0 | H or L position. Don't open circuit. |
| | 1 | 1 | I |

CIRCUIT DESCRIPTION

| Terminal No. | Terminal name | 1/0 | Function |
|-----------------|------------------|-----|---|
| 44 | RA07 | 0 | H or L position. Don't open circuit. |
| 45 | RA08 | 0 | H or L position. Don't open circuit. |
| 46 | RA09 | 0 | H or L position. Don't open circuit. |
| 47 | RA10 | 0 | H or L position. Don't open circuit. |
| 48 | RA11 | 0 | H or L position. Don't open circuit. |
| 49 | RAWE | 0 | H or L position. Don't open circuit. |
| 50 | RACS | 0 | H or L position. Don't open circuit. |
| 51 | C4M | 0 | Crystal dividing output 1 = 4 2336 MHz |
| 52 | Vss | - | GND (0 V) |
| 53 | XTAi | 1 | Crystal oscillator input. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected |
| 54 | OATX | 0 | Crystal oscillator output. f = 8.4672 MHz or 16 9344 MHz depending on the mode selected |
| 55 | MD1 | 1 | Mode select input 1. |
| 56 | MD2 | 1 | Mode select input 2. |
| 57 | MD3 | 1 | Mode select input 3 |
| 58 | SLOB | 1 | Audio data output code select input 2's complement output when "L", offset binary output when "H" |
| 59 | PSSL | ı | Audio data output mode select input. Serial output when "L", parallel output when "H" |
| 60 | APTR | 0 | Aperture compensation control output "H" when R-ch |
| 61 | APTL | 0 | Aperture compensation control output: "H" when L-ch |
| 62 | DA01 | 0 | DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L" |
| 63 | DA02 | 0 | DA02 output when PSSL = "H", C1F2 output when PSSL = "L" |
| 64 | DA03 | 0 | DA03 output when PSSL = "H", C2F1 output when PSSL = "L" |
| 65 | DA04 | 0 | DA04 output when PSSL = "H", C2F2 output when PSSL = "L" |
| 66 | DA05 | 0 | DA05 output when PSSL = "H", C2FL output when PSSL = "L" |
| 67 | DA06 | 0 | DA06 output when PSSL = "H", C2PO output when PSSL = "L" |
| 68 | DA07 | 0 | DA07 output when PSSL = "H", RFCK output when PSSL = "L" |
| 69 | DA08 | 0 | DA08 output when PSSL = "H", WFCK output when PSSL = "L" |
| 70 | DA09 | 0 | DA09 output when PSSL = "H", PLCK output when PSSL = "L" |
| 7.1 | DA10 | 0 | DA10 output when PSSL = "H", UGFS output when PSSL = "L" |
| 72 | DA11 | 0 | DA11 output when PSSL = "H", GTOP output when PSSL = "L" |
| 73 | Voo | | Power supply (+5 V) |
| 74 | DA12 | 0 | DA12 output when PSSL = "H", RAOV output when PSSL = "L" |
| 75 | DA13 | 0 | DA13 output when PSSL = "H", C4LR output when PSSL = "L" |
| 76 | DA14 | 0 | DA14 output when PSSL = "H", C210 output when PSSL = "L" |
| 77 | DA15 | 0 | DA15 output when PSSL = "H", C210 output when PSSL = "L" |
| 78 | DA16 | 0 | DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L" |
| 79 | WDCK | 0 | Strobe signal output: 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF |
| 80 | LRCK | 0 | Strobe signal output 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF |

Notes:

C1F1 : Error correction status monitor output for C1 decode.

C2F1: Error correction status monitor output for C2 decode.

C2FL: Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO: C2 pointer signal. Synchronized to the audio data output. RFCK: Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK: Write frame clock output. 7.35 MHz when locked to the crystal line.

PLCK: VCO/2 output. f = 4.3218 MHz when locked to the EFM signal.

UGFS: Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV: ± 4 frame jitter absorption RAM overflow and underflow display output.

C4LR: Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

BLCK: Output of bit clock, 2.1168MHz BLCK: Inverted output bit clock.

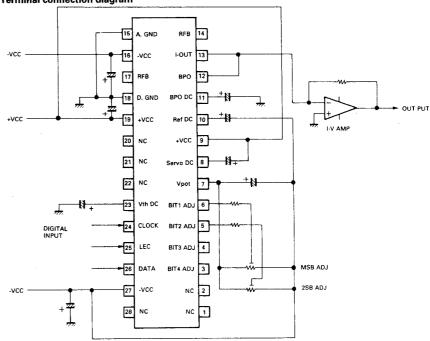
BLCK : Inverted output bit clock.

DATA: Audio signal serial data output.

CIRCUIT DESCRIPTION

9. 18bit serial input D/A converter PCM1701 (X32-1500-11 : IC6, 7)

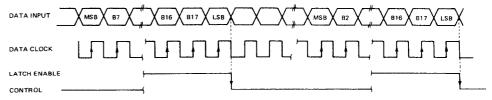
9-1. Terminal connection diagram



9-2. Terminal connections

| Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---------|------------------|---------|---------------------|---------|-------------|
| 1 | NC | 11 | BPO Filter | 21 | NC |
| 2 | NC | 12 | Bipolar offset | 22 | NC |
| 3 | Bit 4 ADJ | 13 | Power supply output | 23 | VTH filter |
| 4 | Bit 3 ADJ | 14 | RF | 24 | Clock input |
| 5 | Bit 2 ADJ | 15 | Analog common | 25 | LEC input |
| 6 | Bit 1 ADJ | 16 | -Vcc | 26 | DATA input |
| 7 | V POT | 17 | RF | 27 | -Vcc |
| 8 | Servo filter | 18 | Digital common | 28 | NC |
| 9 | +Vcc | 19 | +Vcc | | |
| 10 | Reference filter | 20 | NC | | |

9-3. Timing chart



- The data format is of 2's complement, right-justified or continuous data of MSB first.
- Data is taken in to the shift register at the rise of the data clock pulse.

CIRCUIT DESCRIPTION

10. 8x over-sampling digital filter SM5818AP (X32-1500-11 : IC9)

10-1. Function

- 2-channel processing
- 8x over-sampling (interpolation) filter (hereinafter referred to as 8fs for short)
- Serial input data 2's complement, MSB first 16-bit
- Serial output data MSB first 2's complement/COB selectable Selectable between 16-, 18- and 20-bit
- Jitter-free Prevents any faulty operation due to the jitter of the

input clock signal, thus eliminating the jitter transmission over to the output.

- System clock pulse
- Selectable from 192fs, 256fs, 384fs and 512fs
- · Crystal oscillation circuit incorporated
- I/O TTL compatible
- 5 V single power supply
- 28-pin plastic DIP

10-2. Filter configuration

Interpolation filter

Linear phase FIR filter 3-stage configuration First stage (fs — 2fs), 153rd Second stage (2fs - 4fs), 29th Third stage (4fs - 8fs), 17th

- 22-bit filter coefficient, 20x22 bit parallel multiplier/25bit accumulator high-accuracy operation
- · Overflow limiter incorporated

10-3. Applications

- CD playback
- DAT playback
- PCM playback

10-4. Filter characteristics

| Characteristic item | Performance |
|-------------------------|---------------------|
| Pass band | 0 ~ 0.4535fs |
| Reject band | 0.5465fs ~ 7.4535fs |
| Pass band ripple | Within ±0.00005dB |
| Reject band attenuation | More than 110dB |
| Group delay time | Fixed |

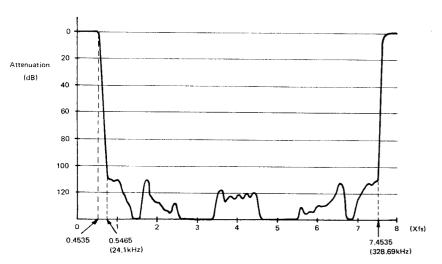
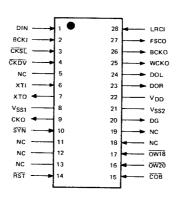


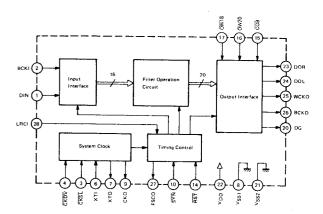
Fig. 8 Frequency response

CIRCUIT DESCRIPTION

10-5 Terminal connection diagram



10-6 Block diagram



10-7. Explanation of terminals

| Pin No. | Pin Name | 1/0 | 'fs' occurring in the description means the sampling frequency of the input data Function |
|--------------------|------------|-----|--|
| 1 | DIN | 十 | Input data. |
| 2 | BCKI | 1 | Input data beat clock pulse. |
| 3,4 | CKSL, CKDV | Ti | XTI pin input frequency selection. (For details, refer to the description of XTI pin.) |
| 5 | NC | 1- | Unused. |
| 6 | XTI . | ' | Oscillator section input pin. 192 fs : CKSL = "H", CKDV = "H" 256 fs CKSL = "H", CKDV = "L" |
| ~ | | | 384 fs : CKSL = "L", CKDV = "H" 512 fs : CKSL = "L", CKDV = "L" |
| - 7 - 8 | XTO | 0 | Oscillator section output pin. |
| | Vssı | ~ | GND1. |
| 9 | CKO | 0 | Oscillator section output clock pulse. (Frequency is the same as in XTI pin.) |
| 10 | SYN | 1 | Jitter-free mode/compulsory sync mode selection. ("H: Jitter-free mode, "L": Compulsory sync mode) |
| 11~13 | NC NC | _ | Unused. |
| 14 | RST | | System reset. ("H" : normal operation, "L" : system reset) |
| 15 | COB | | 2's complement/COB selection. ("H" : 2's complement, "L" : COB) |
| 16,17 | OW20, OW18 | 1 | Number-of-output-bits selection. No. of output bits 16 18 20 OW18 H L H OW20 H H L |
| 18,19 | NC | - | Unused, |
| 20 | DG | 0 | Deglitch control clock pulse. |
| 21 | Vss2 | - 1 | GND2. |
| 22 | VDD | - | Power supply (+5V). |
| 23 | DOR | 0 | Rch 8x over-sampling output data. |
| 24 | DOL | 0 | Lch 8x over-sampling output data. |
| 25 | WCKO | 0 | Output data word clock pulse. |
| 26 | BCKO | 0 | Output data bit clock pulse. |
| 27 | FSCO | 0 | fs-period internal operation timing clock pulse. |
| 28 | LRCI | 1 | Input data sampling rate (fs) clock pulse. ("H": Lch, "L": Rch) |

CIRCUIT DESCRIPTION

10-8, Function

· 8x over-sampling (interpolation) filter function

This function works to output the over-sampling data of sampling rate 8fs. In this case, sampling noises between 0.5465fs (24.1kHz) and 7.4535fs (328.69kHz) are removed.

The interpolation operation block configuration of this LSI is of a cascade connection of three 2x interpolation filters (FIR)

System clock (XTI, XTO, CKO, CKSL, CKDV)

The system clock pulse can be selected from 192fs, 256fs, 384fs and 512fs. More, operation is feasible even by an external clock (input to pin XTI) or a crystal oscillator (inserted between pins XTI and XTO). In this unit, a clock pulse of 8.4672 MHz is input to pin XTI.

From pin CKO, the system clock pulse is output. (See Figure 10-3.) $\,$

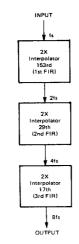


Fig. 9 Configuration of basic operation section

| CKDV CKSL | | H | 1 | | L |
|---------------------------------------|----------------|-------|-------|-------------------------------------|-------|
| | | Н | L | Н | L |
| XTI input clock frequency (Fxi) | Fxi = 1/tXI | 192fs | 256fs | 384fs | 512fs |
| Clock pulse input method | | | | XTI) or internal I between pin X | |
| Internal system clock pulse period | Tsys | t | ΧI | 2* | tXI |

tXI stands for the XTI input clock pulse period

Table 10-1 System clock frequency selection and internal system clock

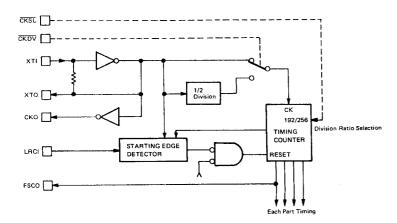


Fig. 10 Clock generation circuit

CIRCUIT DESCRIPTION

· Auto data input (DIN, BCKI, LRCI)

The input data is handled as being of 2's complement, MSB first. Each bit of the serial data input to pin DIN is read in to register SIPO (serial/parallel conversion register) a the leading edge of bit clock pulse BCKI, in which it is in turn converted into a parallel data. The output of SIPO is transferred to each of the Lch and Rch input registers at the trailing/leading edge of clock pulse LRCI.

In addition, the operation section and the output section are independent in signal timing from the input section and are therefore unsusceptible to the jitter of the input section. (Jitter-free mote: For details, refer to the description occurring later.)

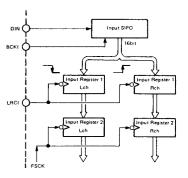
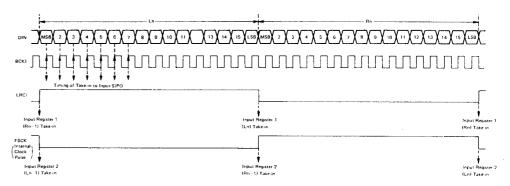


Fig. 11 Configuration of audio data input section



16bits right before LRCI edge is taken in as data.

Fig. 12 Audio data input timing example

Selection between jitter-free mode and compulsory sync mode (SYN, FSCO)

The signal timing (internal timing) applied to internal operation or output, that is produced from the system clock pulse (input to pin XTI), is independent from that of the data input section (BCKI, LRCI).

For this internal timing, the method of countering the jitter of clock pulse input LRCI is available in two types, "jitter-free mode" and "compulsory sync mode". Selection between these both is feasible by setting $\overline{\text{SYN}}$.

1) Jitter-free mode (SYN="H")

As long as the phase difference between clock pulse LRCl and the internal timing is within $\pm 3/8$ to $\pm 3/8$ of the input sampling period (1/fs), the internal timing is not adjusted. Accordingly, even with a jitter component in clock pulse LRCl, the internal timing is not affected so that it is free from faulty operation or jitter transmission to output.

When the phase difference is without the above range, the internal timing is put in phase synchronously with the start side of clock pulse LRCI. More, this treatment is also performed when the reset input is given.

2) Compulsory sync mode (SYN="L")

When this mode is engaged, the internal timing is always reset at a pulse edge of the start side of input LRCI. In this case, when a pulse period shorter than the specified system clock pulse period exists due to the jitter of input LRCI, a faulty operation may result.

Conversely, when a pulse period longer exists, the operation is properly made but no equal output timing is obtained.

3) Clock pulse FSCO (output)

This is a clock pulse with a period of fs obtained from the dividing process of clock pulse XTI.

DP-7020

CIRCUIT DESCRIPTION

Data and DAC control signal output (DOL, DOR, BCKO, WCKO, DG, COB, OW18, OW20)

1) Output data format

1) MSB first

2) 2's complement/COB (Complemented Offset Binary) selection (COB)

2's complement format (COB="H")
COB format (COB="L")

2) Output data number-of-bits selection (OW18, OW20)

As to the number of bits for the output data, any of 16, 18 and 20-bit can be selected.

16-bit output (OW18="H", OW20="H") 18-bit output (OW18="L", OW20="H") 20-bit output (OW18="H", OW20="L")

However, this unit is set at the 18-bit output mode.

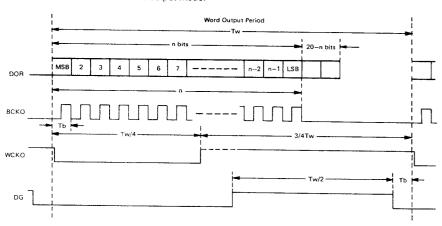
3) Output timing

The output timing of the audio output section is determined according to each internal system clock pulse frequency.

| Item | Symbol in | CKSL | | |
|---------------------------------------|-----------|---------|---------|--|
| - TOTAL | diagram | Н | L | |
| Internal system clock pulse frequency | | 192fs | 256fs | |
| Bit clock pulse period | Ть | Tsys | Tsys | |
| Data word length | Tw | 24*Tsys | 32*Tsvs | |

Tsys: internal clock pulse period (Refer to Table 10-1.)
Tb, Tw: serial output timing (Refer to Figure 13.)

Table 10-2 Output timing



Note: n means the number of output word bits.

Fig. 13 Output timing

· System reset (RST)

When the reset input is made in the jitter-free mode, the internal operation timing is reset in synchronization with the leading edge of input LRCI. Making use of this, the output timing in the jitter-free mode can be aligned with input LRCI.

In the compulsory sync mode, no system reset is needed. Even in the jitter-free mode, the output timing does not need to be aligned with input LRCI and no system reset is necessary.

For system reset at power ON, externally connect a capacity of around 100pF to pin RST. (Figure 10-7)

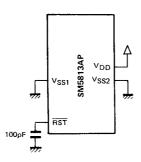
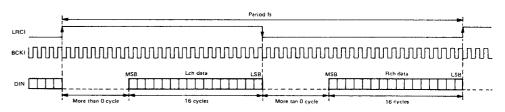


Fig. 14 Circuit example of system reset at power ON

CIRCUIT DESCRIPTION

10-9. Timing chart

• Serial input timing (DIN, BCKI, LRCI)



Note: BCKI should have 18 cycles or more for one word.

Fig. 15 Serial input timing

• Serial output timing (DOL, DOR, BCKO, WCKO, DG)

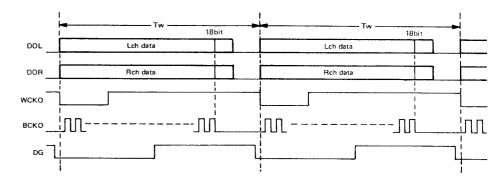


Fig. 16 Serial output timing

CIRCUIT DESCRIPTION

11. D.P.A.C IC KAG01 (X32-1500-11: IC13)

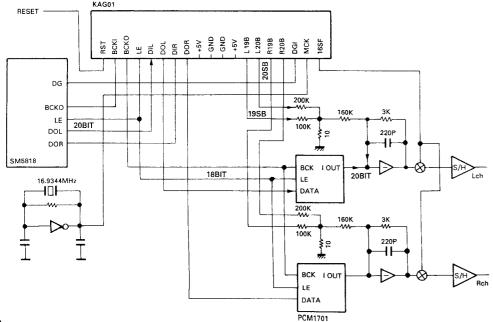
11-1. Terminal connection diagram

| | Г | | 1 |
|------|----------|----|---|
| RST | \dashv | 1 | |
| BCKI | \dashv | 2 | |
| вско | | 3 | l |
| LΕ | - | 4 | |
| DIL | | 5 | |
| DOL | | 6 | ĺ |
| DIR | \dashv | 7 | |
| DOR | \dashv | 8 | 1 |
| +5 | - | 9 | l |
| GND | - | 10 | |
| | | | İ |
| GND | | 11 | l |
| +5 | _ | 12 | ĺ |
| L19B | | 13 | |
| L20B | | 14 | |
| R19B | | 15 | 1 |
| R20B | | 16 | |
| GND | | 17 | l |
| +5 | _ | 18 | ĺ |
| DGI | | 19 | |
| MCK | | 20 | 1 |
| 16FC | | 21 | l |
| | | | |

11-2. Explanation of terminals

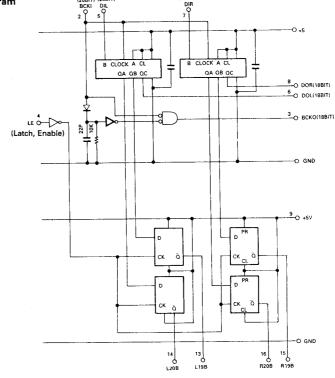
| Pin NO. | Pin Name | Function | | |
|---------|----------|---|--|--|
| 1 | RST | Reset input. | | |
| 2 | BCKI | Bit, Clock input (20bit). | | |
| 3 | BCKO | Bit, Clock output (18bit). | | |
| 4 | LE | Latch, Enable. | | |
| 5 | DIL | L-ch data input (20bit). | | |
| 6 | DOL | L-ch data output (18bit). | | |
| 7 | DIR | R-ch data input. | | |
| 8 | DOR | R-ch data output. | | |
| 9 | +5 | | | |
| 10,11 | GND | | | |
| 12 | +5 | | | |
| 13 | L19B | L-ch 19bit Data output. (complement output) | | |
| 14 | L20B | L-ch 20bit Data output. (complement output) | | |
| 15 | R19B | R-ch 19bit Data output. (complement output) | | |
| 16 | R20B | R-ch 20bit Data output. (complement output) | | |
| 17 | GND | | | |
| 18 | +5 | | | |
| 19 | DGI | Input of D-guritch output of digitaifilter. | | |
| 20 | MCK | 16.9344MHz input. | | |
| 21 | 16FS | 16x D-guritch output. | | |

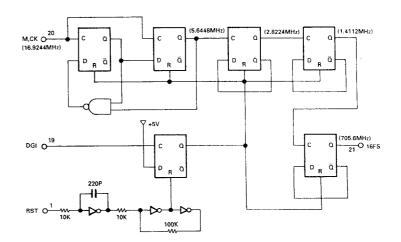
11-3. Block diagram



CIRCUIT DESCRIPTION







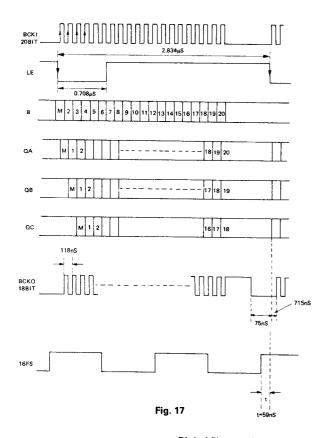
CIRCUIT DESCRIPTION

TBC function

The write data clock pulse (WFS) and the read data clock pulse (RFS) are independent in operation from each other. Thus, the jitter margin ranges ± 1 clock pulse widths.

For 2MSB detection, the level (2's complement) of the 2MLSB detection value at playback is output for both Lch and Rch.

Figure 17 shows the I/O waveforms in use of each digital filter.



· PLL function

Since the phase comparator is of a well-known system, its description is not made here.

For the counter setting of the divider, the type of the input clock pulse, LPF and VCXO circuit configuration, etc., refer to "11-3 Block diagram" and "11-2 Pin functions".

· Digital filter mode setting

Only two modes are available, 16-bit and 18-bit modes. This unit is set at the 18-bit mode.

The mode change is performed at the time of muting. The status right before the cancel of muting is held.

MECHANISM OPERATION DESCRIPTION

Mechanism Operation Description

Fig. 1 shows the relationship of mechanisms in the STOP mode. The OPEN/CLOSE operation of the mechanism and the UP/DOWN operation of the pickup chassis when loading the disc are description below.

Note 1: The black arrow (OPEN) and the white arrow (CLOSE) in the operation description have the following meanings:

Black arrow (OPEN): Tray opening direction

(Tray OPEN)

White arrow (CLOSE): Tray closing direction (Tray CLOSE)

Note 2: Figures in the bracket () in the operation description or accompanied with the part name in the diagram show the reference numbers in the Exploded View.

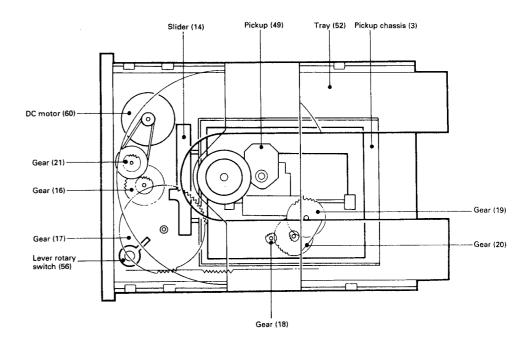


Fig. 1 Tray closed status

MECHANISM OPERATION DESCRIPTION

1. Tray OPEN/CLOSE Operation

By the rotation of the motor (1), the gear (2) is rotated and the tray starts OPEN/CLOSE (3) operation. The OPEN/CLOSE operation stops when the protrusion of the gear comes in contact with the detection switch (3).

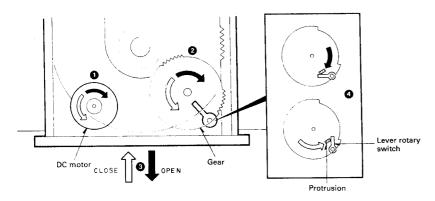


Fig. 2 Tray OPEN/CLOSE operation

2. Pickup Chassis UP/DOWN Movement

Accompanied with the OPEN/CLOSE operation, the lever is shifted (2) by the rotation of the gear (1). Along with the grooves in the lever, the pickup chassis moves up and down (3).

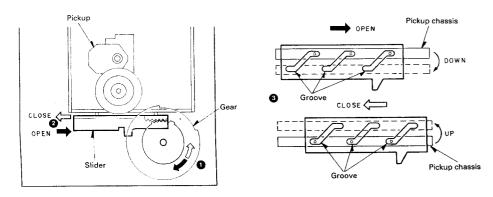
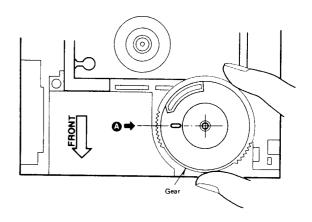


Fig. 3 Pickup chassis UP/DOWN movement

3. Gear Installing Position

When re-installing the gear after removing it, attach the gear at the position (A) shown in the condition when the pickup chassis has been lowered.



MECHANISM OPERATION DESCRIPTION

Fig. 4 Gear installing position

ADJUSTMENT

| \neg | | INPUT | OUTPUT | PLAYER | ALIGNMENT | ALIGN FOR | 21G |
|--------|---------------------------|---|---|--|--------------------------------------|---|-----|
| o. | ITEM | SETTING | SETTING | SETTING | POINT | IIDTOT TOTAL | 10 |
| 1 | LASER POWER | | Apply the sensor section of the optical power meter on the pickup lens. | Short-circuit pins TEST and turn the power on to enter the test mode. Press the MANUAL S. key()M) to move the pickup outwards. Press the CHECK key to check that the LD emits light. Then. | - | On the power from D.1 to 0.3mV, when the diffraction grating is correctly aligned with the RF level of 1.0Vp por more and the TE (servo open) level of 1.0Vp por sore, the pickup | (a) |
| 2 | YCO | | Connect a frequency counter to PLCK | confirm that the display is 03 . Press the STOP key. and confirm that | L4 (X32-1500) | is acceptable. | (ъ) |
| - | | | (X32-1500) | the display is "01". | | ļ | |
| 3 | TRACKING ERROR BALANCE | Test disc Type 4 | Connect an oscilloscope as follows. CH1: RF (X32-1500 RF) CH2: TE (X32-1500 TP3) | Press the REPEAT key to open the tray. Load a disc and close the tray by pushing it by hand. Then, press the CHECK key. Confirm that the display is "03". | TE BALANCE VRIO4 (X32-1500) | Symmetry between upper and lower patterns. or DC=0±0.03¥ | (e) |
| 4 | FOCUS ERROR BALANCE | Test disc Type 4 | Connect an oscilloscop as follows: CH1: RF (X32-1500 RF) CH2: TE (X32-1500 TP3) | Press the PLAY key. Confirm that the display is 05 ". | FE BALANCE VR103 (X32-1500) | Optimum eyepattern | (d |
| 5 | FOCUS GAIN | Test disc Type 4 Apply signal of 800Hz, 50Vrms to CN10 pin 1 2. (X32-1500) | Connect an LPF to CNIC pin 1-2.to which connec an oscilloscope or an AC voltmeter. (X32-1500) | t key. Confirm that the display | FOCUS GAIN VR101 (X32-1500) | Two YTYMs should read the same value. 50m¥rms | (6 |
| 6 | TRACKING GAIN | Tost disc Type 4 Apply signal of 1.0kHz, 50Vrms to CN10 pin 4-5. (X32-1500) | Connect an LPF to CN1 pin 4-5.to which conne an oscilloscope or an AC voltmet (X32-1500) | ct key. Confirm that the display | TRACKING GAIN VRIO2 (X32~1500) | Two YTYMs should read the same value. 50m¥rms | (|
| 7 | DAC DISTORTION (MSB) | Test disc Type 4 | Connect an distortion meter to the output terminal(FIXED). | Play the 1kHz, -20dB signal in track No.15 | VR1:Lch VR2:Rch (X32-1500) | Minimum distortion | , |
| 8 | DAC DISTORTION (2SB) | Test disc Type 4 | Connect an distortion meter to the output terminal(FIXED). | Play the 100Hz, OdB signal in track No.4. | YR9:Leh YR10:Reh (X32-1500) | Minimum distortion | |

(Note) Type 4 disc: SONY YEDS-18 Test Disc or equivalent.

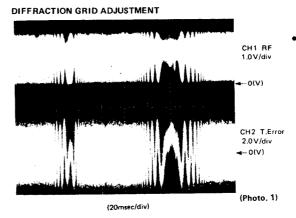
1,PF: Around 47k9 + 390pF or so.

Step 1-6 are in TEST mode.

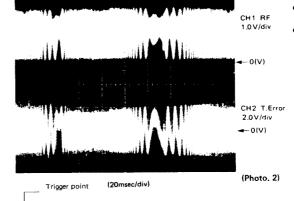
If adjust step 7 or 8, shold readjust steps 7 and 8.

DP-7020(K)

ADJUSTMENT

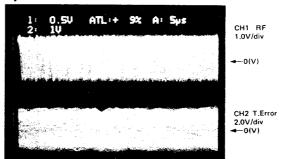


 RF signal and T.Error signal after diffraction grating adjustment.



- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.





--- Projection

(5µsec/div)

(Photo, 3)

- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observies in the T.Error waveform.

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ADJUSTMENT

CH1 RF 0.5V/div CH2 E.Spot 0.1V/div AC coupling for CH2 only

(2µsec/div)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 20 µs after RF signal, in the form of a projection.

CH1 RF 1.0V/div CH2 T.Error 2.0V/div

(Photo, 5)

(Photo, 4)

- RF signal and T.Error signal; in test mode (Focusing) ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR104 of X32-1500)

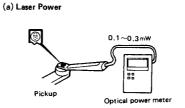
20) 0.50 ATL:+ O% A: Ips RF signal 0.5V/div (Photo. 6)

(1 µse c/div)

(20msec/div)

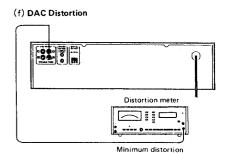
- RF signal in test mode (PLAY).
- · Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.

ADJUSTMENT

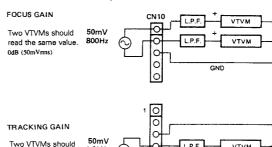


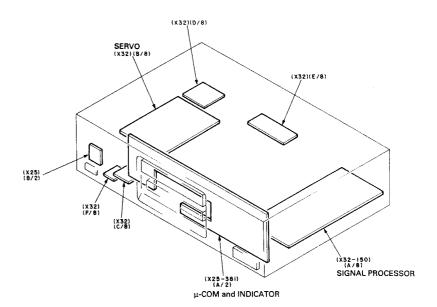
1.0kHz

read the same value. 0dB (50mVrms)



(e) Focus Gain and Tracking Gain





VTVM

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VOLTAGE TABLE

(X32-1500-11)

| IC1 | | IC | :9 | | ı | C12 | | |
|---------|--------|-----|-------|---------------|-----|------|---|---------------|
| 1 | -2.6V | Г | 1 | 0V(2.8V) | [| 1 | Ţ | -5.6V |
| 2,3 | 0V | - | 2 | 3.4V | l | 2,3 | 1 | 0V |
| 4 | -16.2V | Т | 3 | 5.0V | | 4 | 7 | -10.5V |
| 5,6 | 5.6V | F | 4,5 | 0V | | 5.6 | 7 | 5.0V |
| 7 | 2.0V | ۲ | 6 | 3.2V | | 7 | 7 | 5.7V |
| 8 | 15.6V | | 7 | 2.7V | li | 8 | | 9.0V |
| 1C2,3 | | Г | 8 | 0V | li | C13 | | |
| 1~3 | ov | | 9 | 3.1V | | 1 | | 5.0V |
| 4 | -10.4V | Ŀ | 10~13 | 0V | | 2 | ╗ | 2.8V |
| 5~7 | ov | Γ | 14,15 | 5.0V | | 3 | | 3.1 |
| 8 | 10.5V | Γ | 16 | OV | 1 | 4 | ٦ | 4.0V |
| IC4 | | Γ | 17 | 5.0V | | 5~8 | | 0V |
| 2,3 | 0V | Γ | 18,19 | 0V | | 9 | | 5.0V |
| 4 | -10.4V | Γ | 20 | 2.9V |]] | 10,1 | 1 | OV |
| 5~7 | 0V | | 21 | 0V | | 12 | | 5.0V |
| 8 | 10.5V | Γ | 22 | 5. 0 V | 1 | 13 | | 3.8V |
| IC5 | | П | 23,24 | 0V | 1 | 14 | | 5.0V(3.8V |
| 1~3 | 0V | | 25 | 4.0V |] | 15 | | 3.8V |
| 4 | -10.4V | | 26 | 2.8V | 1 | 16 | | 5.0V(3.8V |
| 5~7 | 0V | | 27,28 | 2.5V |] | 17 | , | 0V |
| . 8 | 10.5V | H | C10 | | | 18 | | 5.0V |
| IC6,7 | | | 1~6 | 3.3V | | 19 | | 4.0V |
| 1.2 | 0V | | 7 | 0V | | 20 | | 3.3V |
| 3 | -9.5V | | 8 | 3.3V |] | 21 | | 3.2V |
| 4 | -9.6∨ | | 9 | 2.8V | 1 | | _ | |
| 5,6 | -9.7V | | 10~13 | 3.3V | 1 | | | |
| 7(IC6) | -9.0V | | 14 | 5.0V |] | | | |
| 7(IC7) | 9.0V | ı | C11 | | | | | |
| 8 | 1.7V | ١٢ | 1 | OV | 34 | ~40 | _ | 0V |
| 9 | 5.0V | [| 2 | 0V(5.0V) | Г | 51 | | 3.3V |
| 10 | -4.3V | | 3 | 0V(2.5V) | | 52 | | 0V |
| 11 | 3.3V | | 4 | 0V(2.8V) | Γ | 53 | | 3.1V |
| 12~18 | 0V | 1 | 5 | 0V(3.0V) | | 54 | | 2.3V |
| 19 | 5.0V | [| 6 | OV(2.9V) | 5! | 5,56 | | ٥٧ |
| 20~22 | 1.0V | l | 7 | 0V(5.0V) | Г | 57 | | 5.0V |
| 23 | 3.3V | { | 8 | 2.4V | 5 | 8,59 | | 0V |
| 24 | 3.0V | 1 | 9 | 3.3V | 6 | 5,66 | | 1.9V(0V) |
| 25 | 4.0V |] [| 10 | 0V | Т | 67 | | 5.0V(0V) |
| 26 | 0V | } | 11 | 2.5V | T | 68 | 1 | .0V(2.5V) |
| 27(IC6) | -11.0V |] [| 12 | ٥٧ | Т | 69 | | 2.5V |
| 27(IC7) | 11.0V |] [| 13~16 | 5.0V | Т | 70 | Γ | 3.3V |
| 28 | OV | | 17 | 0V | Т | 71 | Γ | 5.0V |
| IC8 | | | 18,19 | 0V(0.5V) | T | 72 | | 5.0V(0V) |
| . 1 | 5.6V |) | 20~24 | ٥٧ | T | 73 | _ | 5. 0 V |
| 2,3 | 5.0V | 1 | 25 | 2.5V | 1 | 74 | | 5.0V(0V) |
| 4 | -10.5V |] | 26 | 0V | Τ | 75 | | 2.6V |
| 5,6 | 5.0V | | 27 | 3.1V | 7 | 6,77 | | 3.2V |
| 7 | 5.6V | | 28~32 | 0V | Т | 78 | | 0V |
| 8 | 9.0V |] | 33 | 5.0V | 7 | 9.80 | | 2.5V |

| 14 | | IC104 | |
|-------|---------------|-------|--------------|
| 1 | OV | 1-3 | OV |
| 2,3 | 2.5V | 4 | 4.6V |
| 4 | -5.0V | 5 | 4.5V(3.6V) |
| 5,6 | 0V(2.6V) | 6 | -5.0V |
| 7 | 0V | 7~14 | 0V |
| 215 | | 15 | -1.0V(-1.7V) |
| 1,2 | 5.0V | 16 | -1.2V |
| 3 | ٥٧ | 17 | -5.0V |
| 4 | 5.0V | 18~20 | OV |
| 5 | 5.0V(2.8V) | 21 | -4.9V |
| 6 | 0V(2.8V) | 22 | 0V |
| 7 | 0V | 23 | -3.5V(-1.8V) |
| 8 | 5.0V(2.8V) | 24,25 | 0٧ |
| 9 | 0V(2.8V) | 26 | OV |
| 10 | 5.0V(0V) | 27 | 4.1V(2.5V) |
| 11 | 5.0V | 28 | 0V(4.8V) |
| 12,13 | 0V | 29 | 4.9V(0V) |
| 14 | 5. 0 V | 30 | 5.0V |
| C101 | | IC105 | |
| 1 | -4.4V | 1-3 | 0V |
| 2,3 | OV | 4 | -0.9 |
| 4 | -9.0V | 5~7 | 0V |
| 5,6 | 4.5V | 8 | 0.9V |
| 7 | 4.7V | IC106 | |
| 8 | 9.0V | 8 | 0V |
| C102 | | 9~11 | 5.0V(2.7V) |
| 1,2 | ٥٧ | 12 | 0V(4.4V) |
| 3,4 | 5.0V | 13 | 4.1V(2.5V) |
| 5 | 5.0V(0V) | IC108 | |
| 6.8 | ٥٧ | 1~3 | 0V(0.8V) |
| 7 | -0.5V | 4 | -0.5V |
| C103 | | 5~7 | 0V |
| 1~4 | 0V | 8 | 5.0V |
| 5 | 5.0V(0V) | IC110 | |
| 6 | 0V | 1~3 | 0V |
| 7 | 4.9V | . 4 | -9.0V |
| 8~10 | 5.0V | 5~7 | 0V |
| 11~13 | 0V | 8 | 9.0V |
| 14 | -4.0V | IC201 | |
| 15 | 5.0V | 1~3 | 0V |
| 16 | OV | 4 | -10.8V |
| 17 | -5.0V | 5~7 | 0V |
| 18 | 2.7V(0V) | 8 | 10.1V |
| 19-25 | 01/ | 1 | |

19-25 0V 26 5.0V 27-30 0V

| | 8 | С | E |
|----------|----------|----------|----------|
| Ω1 | 15.0V | 10.7V | 15.6V |
| Q2 | -16.1V | -10.8V | -15.5V |
| Q3(0N) | -10.5V | 6.3V | -10.5V |
| Q3(OFF) | -5.5V | -10.7V | |
| Q4 | -10.6V | ٥V | -10.8V |
| | (-10.1V) | (-10.7V) | (-10.8V) |
| Q5(ON) | 0.7V | 0V | 0V |
| Q5(OFF) | -10.7V | _ | _ |
| Q6 | | 0V | _ |
| Q7 | 0.7V | -3.0V | OV |
| Q8 | | _ | 0V |
| Q13 | 5.5V | 10.5V | 4.8V |
| Q14 | 3.3V | 10.5V | 5.0V |
| Q16,15 | 5.6V | 9.0V | 5.0V |
| Q17 | -5.6V | -10.5V | -5,0 |
| Q18 | 5.7V | 9.0V | 5.0V |
| Q20 | 4.7V | 0V | 2.3V |
| Q21 | 3.1V | 0V | 2.3V |
| O22 | 0.5V | 0.5V | 5.0V |
| | (0V) | (OV) | - |
| Q101 | 8.5V | 5.0V | 9.1V |
| Q102 | -8.3V | -5.0V | -9.0V |
| Q103 | 5.67 | -14.2V | 5.0V |
| Q104 | -30.6V | -39.5V | -30V |
| Q105 | OV | -9.0V | 0V |
| Q106,114 | 0V | 9.0V | 0V |
| Q111 | ٥٧ | -9.0V | |
| Q112 | 0V | 9.0V | T = |
| Q113,115 | OV | -9.0V | 0V |
| Q116 | OV | 9.0V | ov |
| Q117 | OV | 5.0V | 0V |
| Q118 | 4.5V | 1.3V | 5.0V |
| | (3.6V) | (2.1V) | (4.3V) |

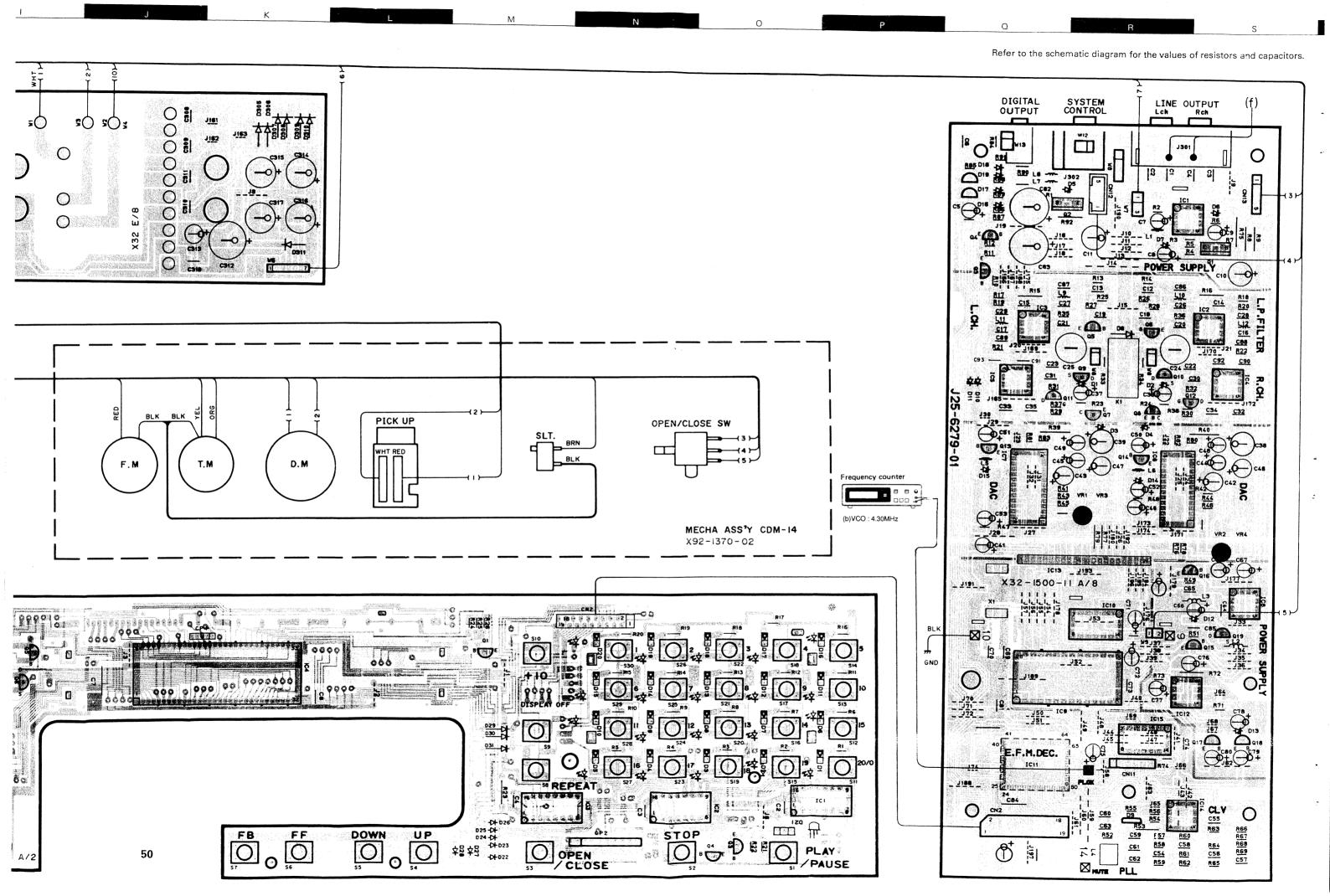
(X25-3810-00)

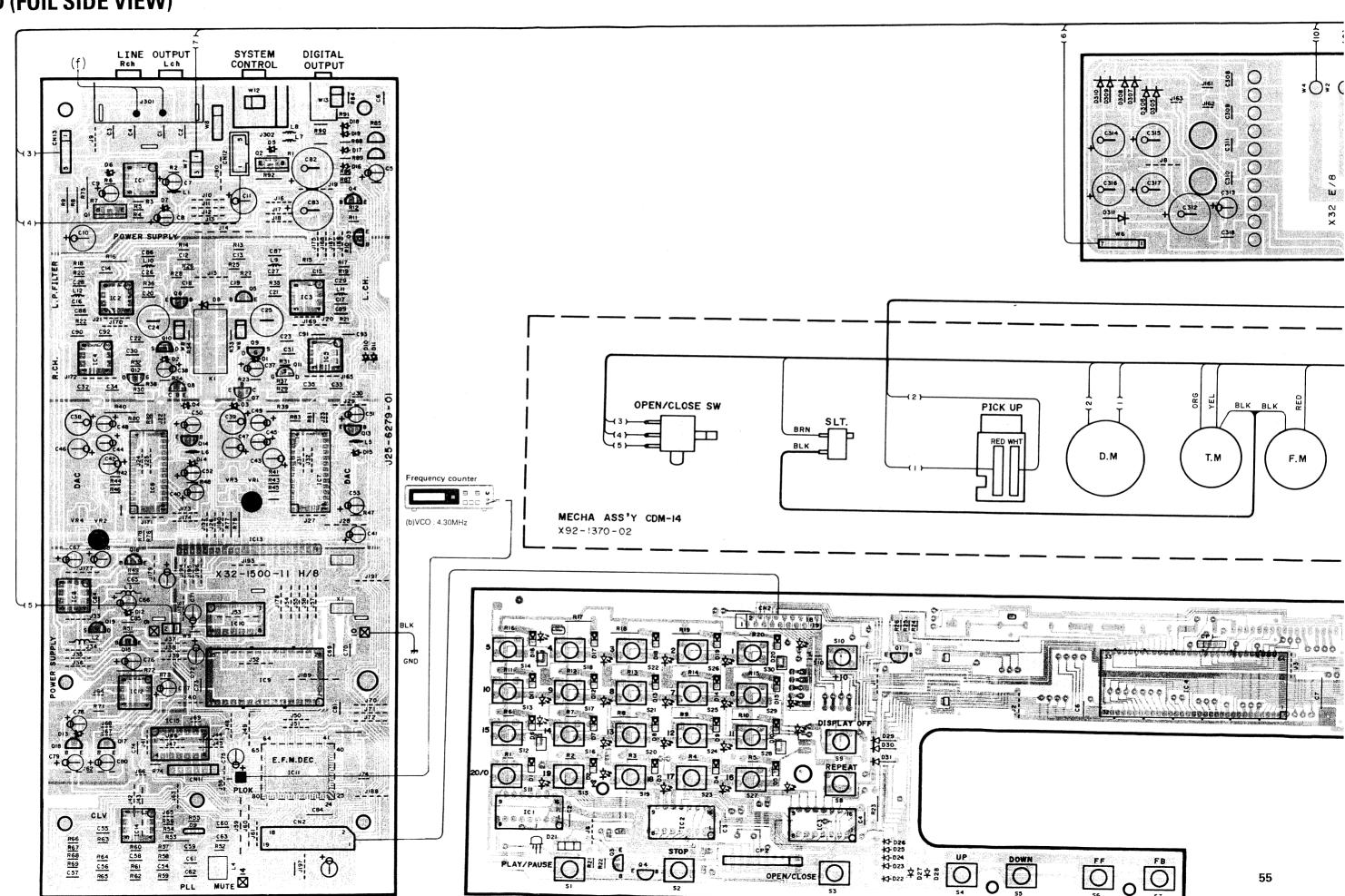
IC1

| - 1 | | 1 | |
|-------|----------|-------|----------|
| 5 | 5.0V(0V) | 25~27 | 5.0V |
| 6 | 2.5V | 28,32 | 0V |
| 7,10 | 0V | 36 | 5.0V(0V) |
| 8,9 | 5.0V | 37.39 | 5.0V |
| 11~13 | 0V(5.0V) | 38 | ٥٧ |
| 14 | 5.0(ON) | 50.51 | 4.9V(0V) |
| | 0V(OFF) | 52,53 | OV |
| 15,19 | 5.0V | 56 | -30V |
| 16~18 | 0V | 57 | -5.0V |
| 20~24 | ٥V | 64 | 5.0V |

| IC2 | |
|-----|------|
| 1,3 | 5.0V |
| 2 | ٥٧ |

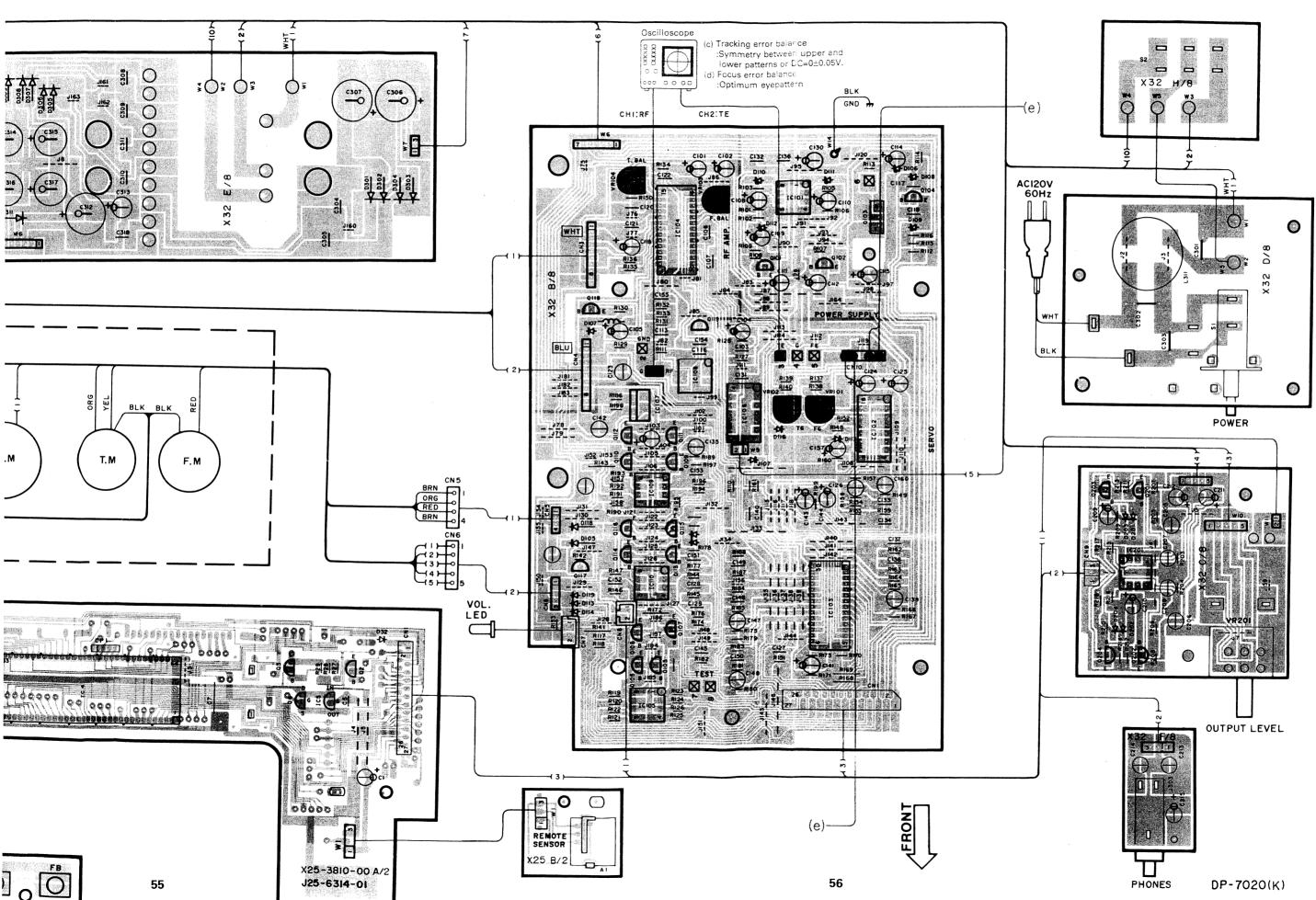
| | В | O | E |
|------|----------|-----------|--------|
| Q1,2 | -26.6V | 5.0V | -26.6V |
| 03 | 5.0V(0V) | 0V(5.0V) | 5.0V |
| Ω4 | 5.0V | -9.0V(0V) | 5.0V |

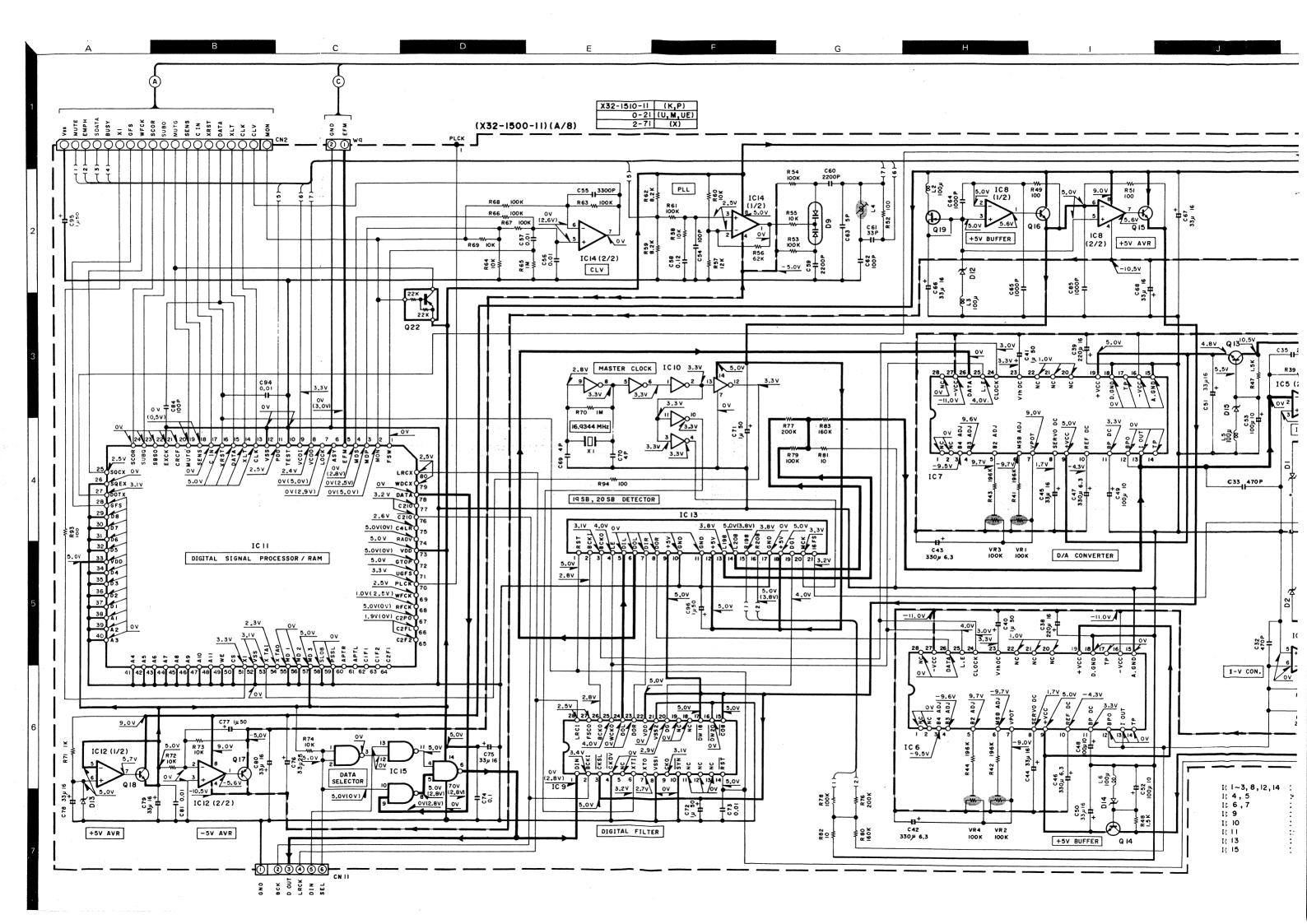


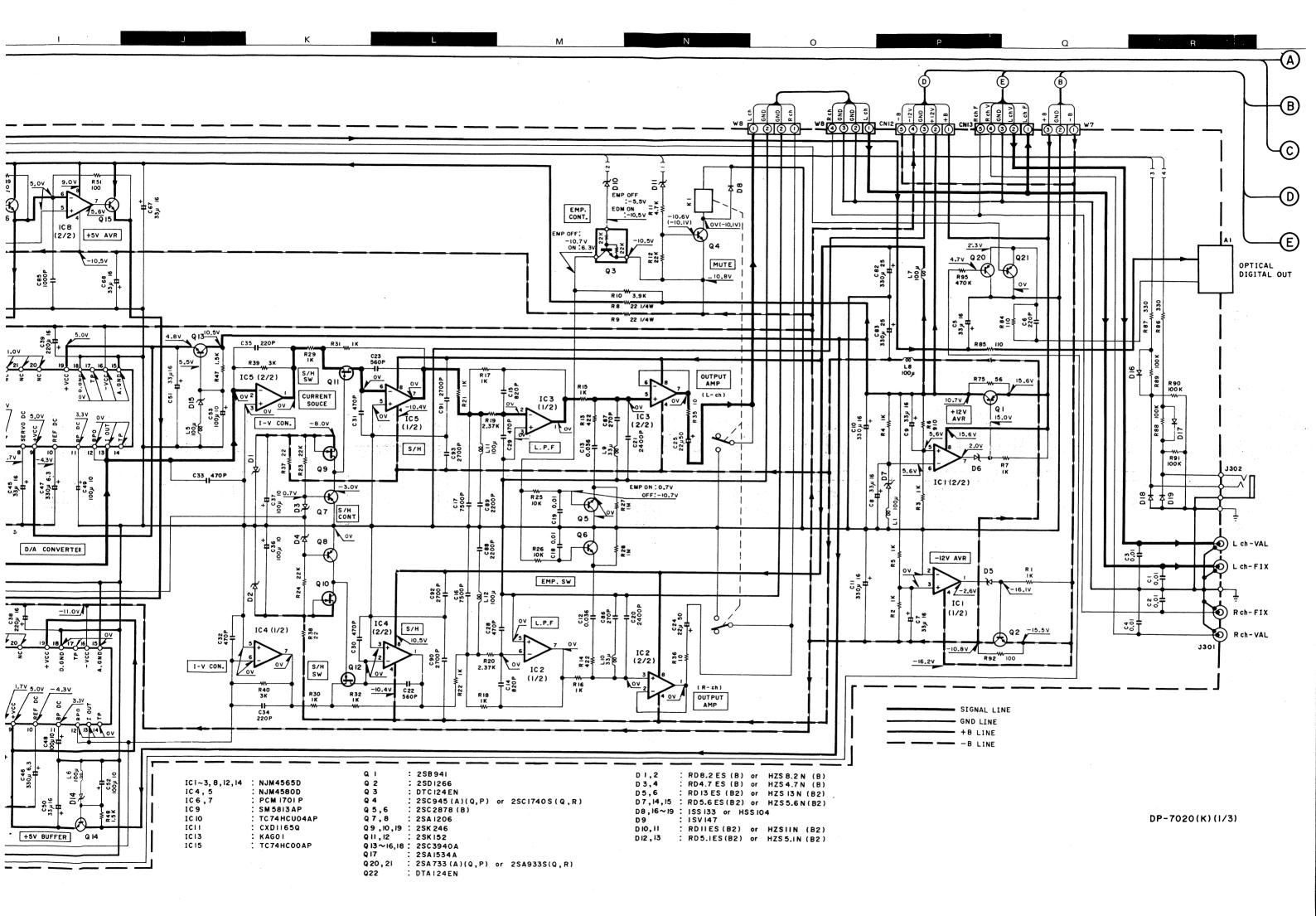


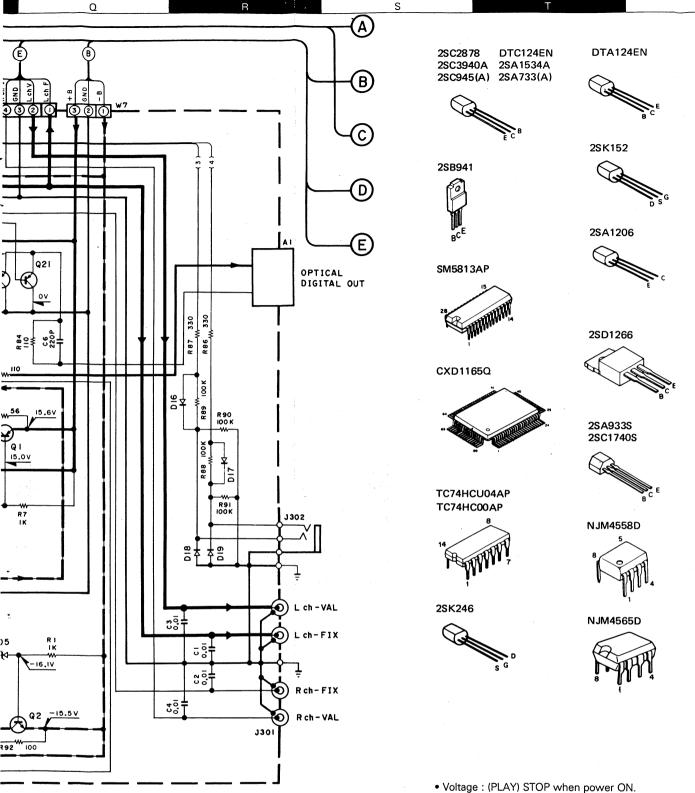
53

Refer to the schematic diagram for the values of resistors and capacitors.









• DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to varations between individual instruments or/and units.

CAUTION: For continued safety, replace safety critical $components \, only \, with \, manufacturer's \, recommendel \, \boldsymbol{\rho} \, arts$ (refer to parts list). \triangle Indicates safety critical components. To reduce the risk of electric shock, leakage-ur rent or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply (in cuit) before the appliance is returned to the customer.

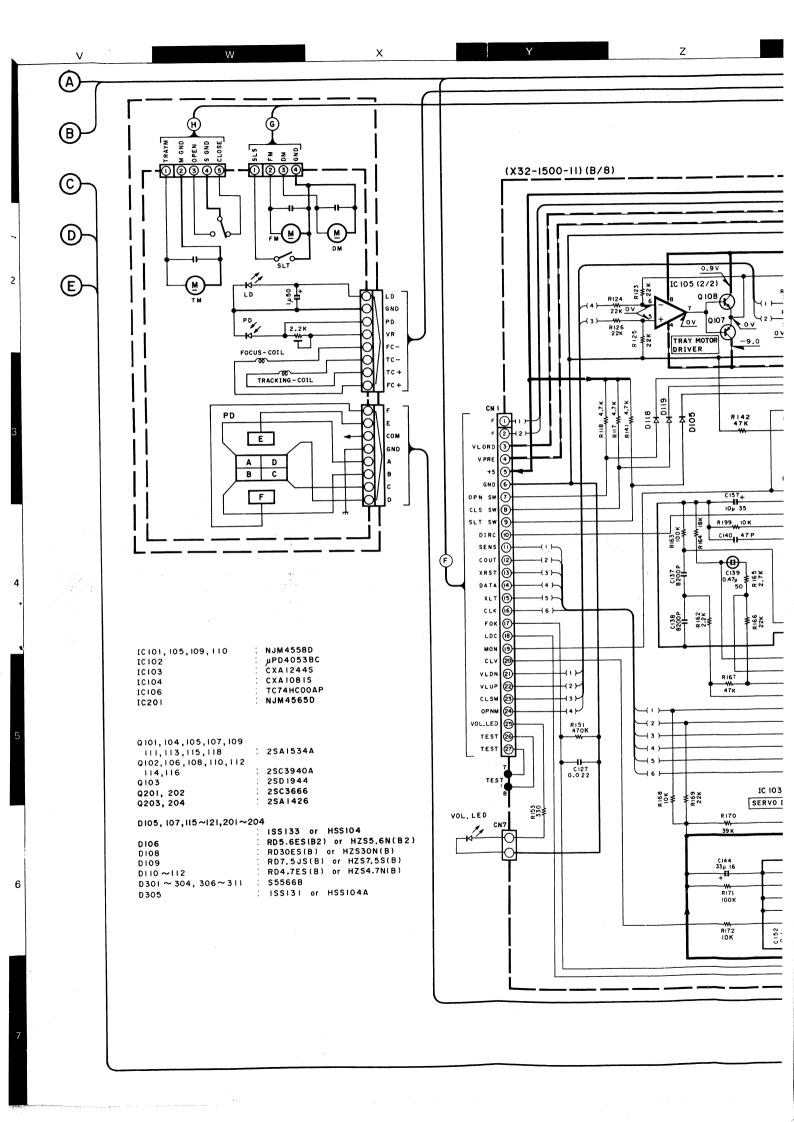
DP-7020(K)(1/3)

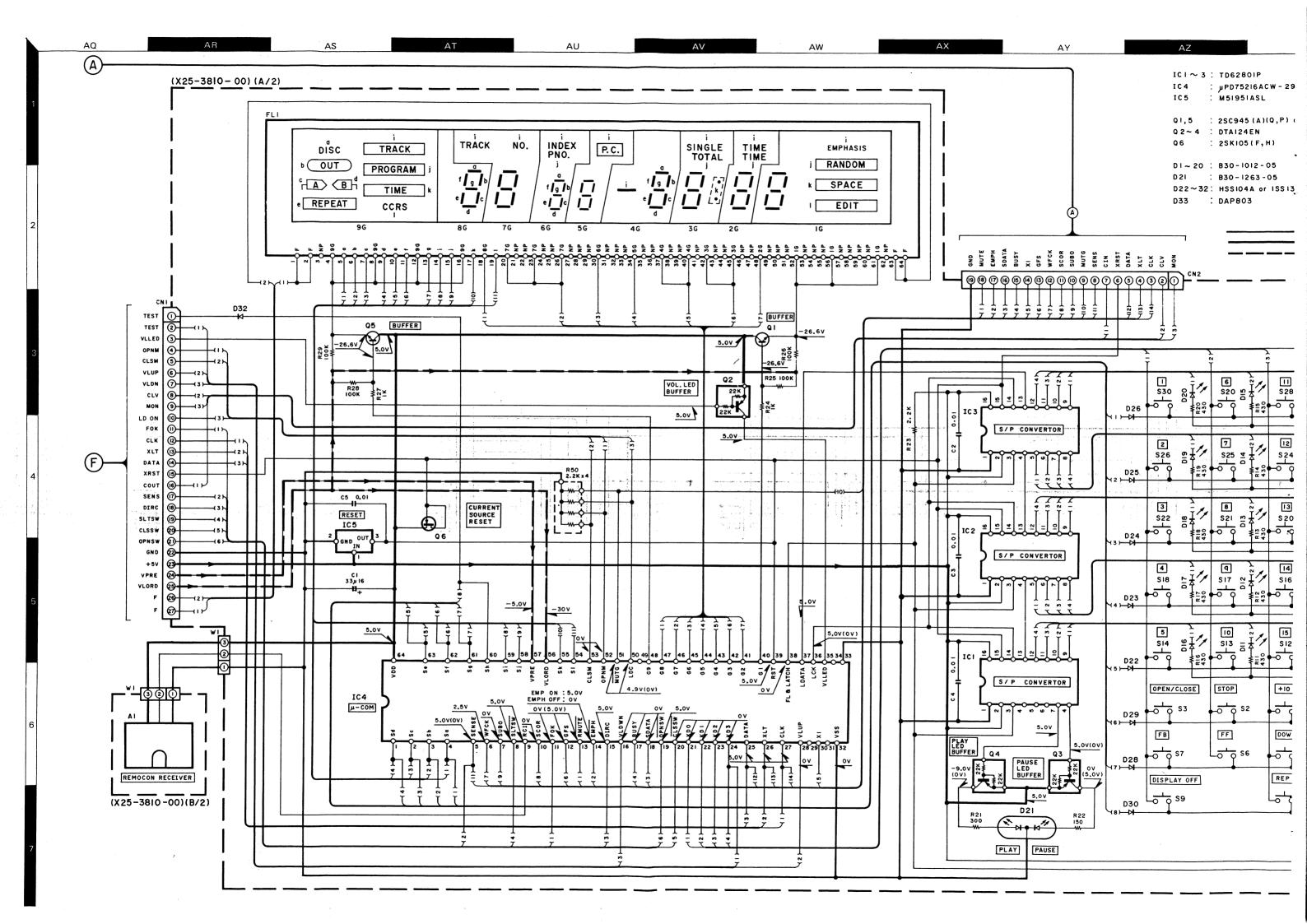
L LINE

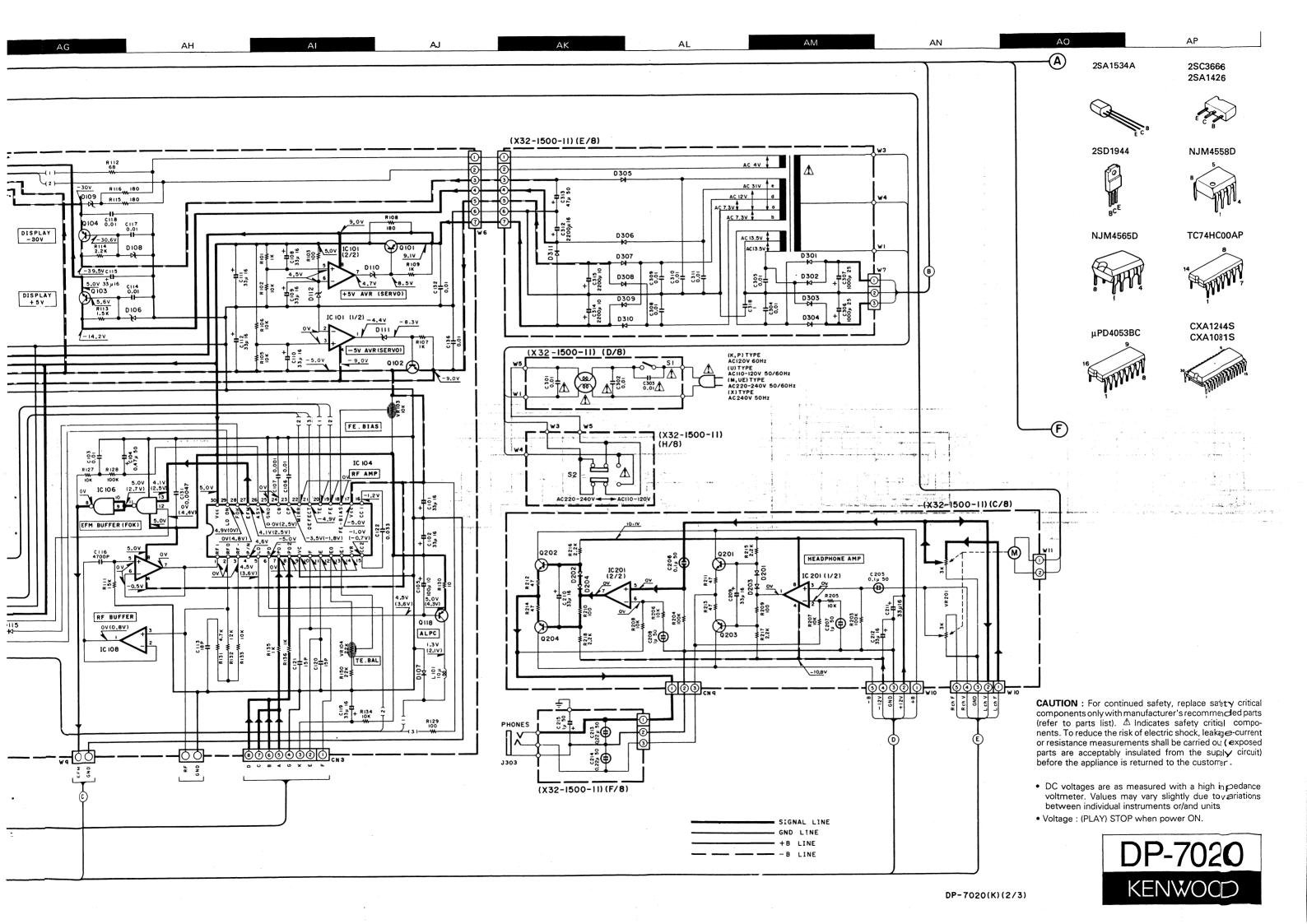
INE

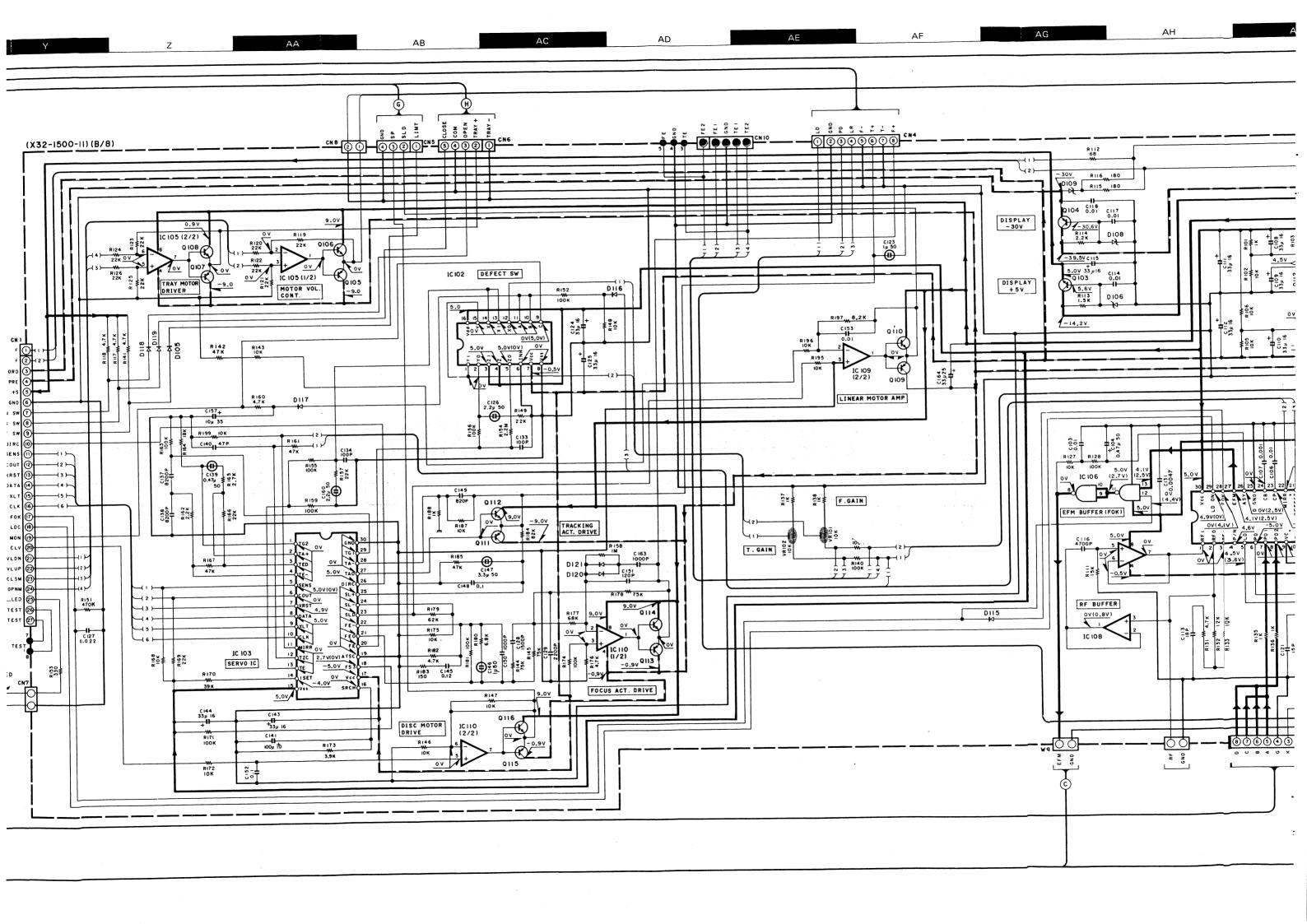
ΝE

NE









BE

вв

TD62801P

μPD75216ACW - 295

M51951ASL

: 2SC945 (A)(Q,P) or 2SC1740S(Q,R)

: DTA124EN

: 2SK105(F,H)

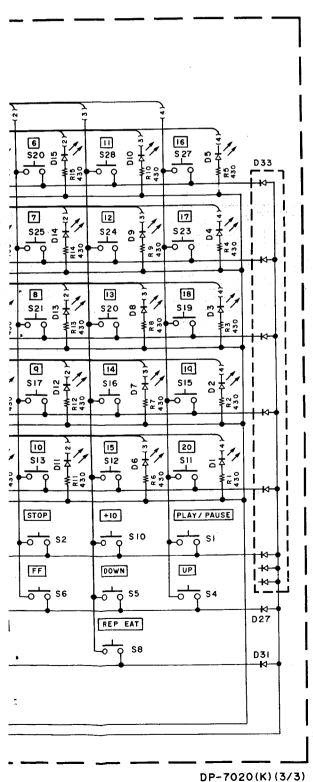
* B30-1012-05

: B30-1263-05

: HSS104A or ISS131

- DAP803

GND LINE +B LINE -B LINE



DTA124EN

вс

μPD75216ACW-295





2SC945



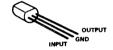


2SK105

2SC1740S



M51951ASL

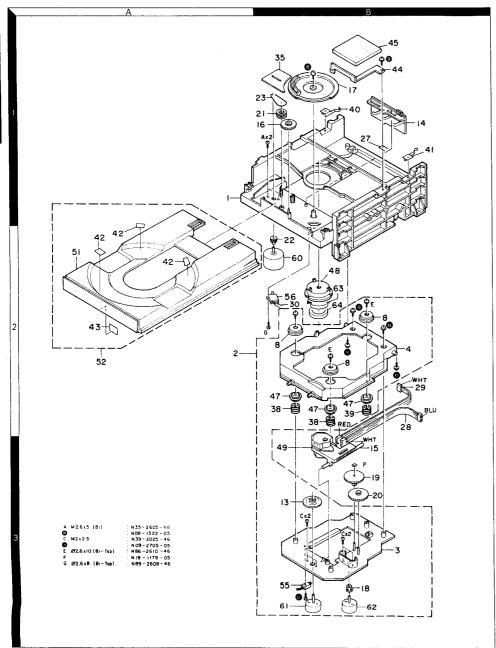


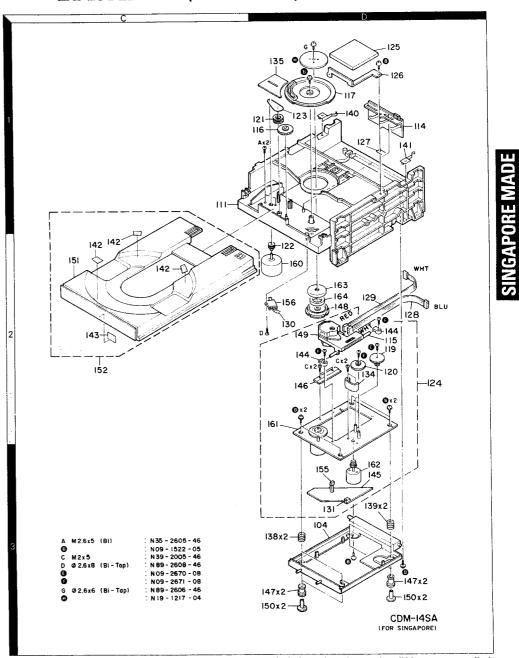
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). A Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Voltage: (PLAY) STOP when power ON.

EXPLODED VIEW (MECHANISM): JAPAN MADE

EXPLODED VIEW (MECHANISM): SINGAPORE MADE

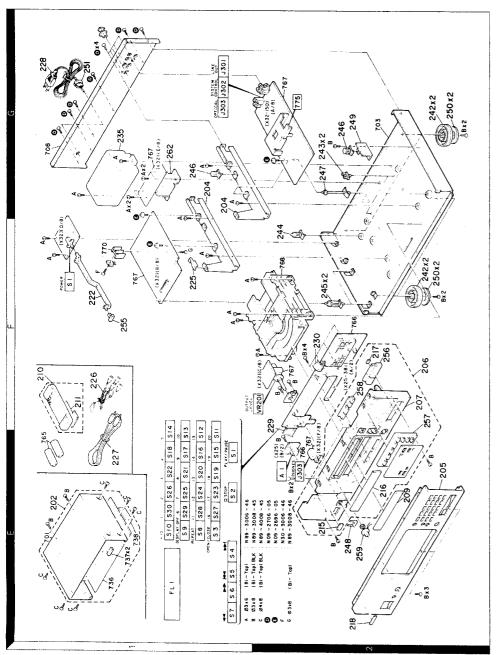




Parts with the exploded numbers larger than 700 are not supplied.

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



PARTS LIST

× New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnes dans le Parts No. ne sont pas fournis.

Telle ohne Parts No. werden nicht geliefent.

| Ref | No. | Addres | s New Parts | Parts No. | Description | Desti- Re- |
|---------------------------------|-----|------------------------------------|----------------|---|---|------------------------|
| 参 | 照番号 | 位置 | | 部品書号 | 部 品 名 / 規 格 | 仕 向備3 |
| | | | | DP-7020 | / JAPAN | |
| 202 204 205 206 207 | | 1E 1G 2E 2F 2F | * * * * | A01-1804-12 A13-1222-03 A20-5899-02 A22-1130-12 A22-1131-01 | METALLIC CABINET ASSY FRAME PANEL SUB PANEL ASSY SUB PANEL | |
| 209 210 211 | | 2E 1F 1F | * | A29-0153-03 A70-0308-05 A09-0078-08 | PANEL(TRAY) REMOCON ASSY(RC-P8020) BATTERY COVER | |
| 215 216 217 218 | | 2E 2E 2E 2E | * | B10-1047-04 B10-1048-03 B12-0066-04 B43-0287-04 B46-0092-03 | FRONT GLASS(REMOCON) FRONT GLASS(DISPLAY) INDICATOR KENWOOD BADGE WARRANTY CARD | к |
| - | | | * | B46-0094-03 B46-0095-03 B46-0096-13 B46-0121-03 B50-9861-00 | WARRANTY CARD WARRANTY CARD WARRANTY CARD WARRANTY CARD INSTRUCTION MANUAL(ENGLISH) | UUE UUE X P |
| - | | | * | B50-9862-00 B50-9863-00 B58-0223-04 B58-0513-04 | INSTRUCTION MANUAL(FRENCH) INSTRUCTION MANUAL(SPANISH) CAUTION CARD (PRE-SET 120V) CAUTION CARD (PRESET220-240) | PM M U UE |
| 222 | | 1F | | D21-1540-03 | EXTENSION SHAFT | |
| 226 227 228 228 228 | | 1E 1F 1G 1G 1G | | E30-0505-05 E30-0977-05 E30-0459-05 E30-0780-05 E30-0812-05 | AUDIO CORD CORD WITH PLUG AC POWER CORD AC POWER CORD AC POWER CORD | M KP U <u>UE</u> |
| 228 229 230 | | 1G 2F 2F | | E30-1341-05 E31-4289-05 E31-4790-05 | AC POWER CORD WIRING HARNESS WIRING HARNESS | х |
| 235 | | 1 G | | F11-0440-03 | SHIELDING CASE | |
| 1111 | | | * * * | H01-8634-04 H10-3894-02 H10-3895-02 H21-0273-04 H25-0232-04 | ITEM CARTON CASE POLYSTYRENE FOAMED FIXTURE(L) POLYSTYRENE FOAMED FIXTURE(R) PROTECTION SHEET PROTECTION BAG (235X350X0.03) | KPU <u>UE</u> X |
| - | | | 1 | H25-0361-04 | PROTECTION BAG | KPU <u>UE</u> X |
| 242 243 244 245 246 | | 2F, 20 2G 2F 2F 1G, 20 | | J02-1052-05 J11-0129-05 J19-0506-05 J19-0581-05 J19-2598-05 | FOOT ASSY WIRE CLAMPER UNIT HOLDER UNIT HOLDER HOLDER | |
| 247 248 249 251 | | 2G 2E 2G 1G | * | J19-3208-05 J21-3326-05 J21-5560-04 J42-0083-05 J61-0307-05 | UNIT HOLDER JACK MOUNTING HARDWARE MOUNTING HARDWARE POWER CORD BUSHING WIRE BAND | |
| 255 256 | | 1F 2F | * | K27-2004-04 K29-3780-04 | KNOB (BUTTON)(POWER) KNOB (PLAY/PAUSE) | |

E: Scandinavia & Europe K: USA

U: PX(Far East, Hawaii) T: England M: Other Areas

UE : AAFES(Europe)

⋆ New Parts

PARTS LIST

Parts without Parts No. are not supplied. Les articles non mentionnes dans le Parts No. ne sont pas fournis.

| | Teile onne Parts | No. werde | n nia | ht gellefert. | | | |
|---|---------------------------------|----------------------------------|--------------|---|---|-------------------------|-------------|
| | Ref. No. | Address | New Parts | Parts No. | Description | | Re- |
| | 参照番号 | 位置 | # | 部品番号 | 部品名/規格 | nation 仕 向 | marks 備考 |
| | 257 258 259 | 2F 2F 2E | * | K29-3782-03 K29-3783-03 K29-3796-05 | KNOB (20KEY) KNOB (SKIP) KNOB ASSY(OUTPUT LEVEL) | | |
| Δ | 262 262 262 | 1G 1G 1G | | L01-5601-05 L01-5602-05 L01-5604-05 | POWER TRANSFORMER POWER TRANSFORMER POWER TRANSFORMER | KP X UM <u>UE</u> | |
| | A B C D E | | * | N89-3006-46 N89-3008-45 N89-4008-45 N09-2706-05 N09-2696-05 | BINDING HEAD TAPTITE SCREW BINDING HEAD TAPTITE SCREW BINDING HEAD TAPTITE SCREW TAPTITE SCREW STEPPED SCREW | | |
| | | , | | DP-7020 / | SINGAPORE | 4 | |
| | 202 204 205 206 207 | 1E 1G 2E 2F 2F | * * * * | A01-1822-02 A13-1240-03 A20-5899-02 A22-1130-02 A22-1131-01 | METALLIC CABINET ASSY FRAME PANEL SUB PANEL ASSY SUB PANEL | | |
| | 209 210 211 | 2E 1F 1F | * | A29-0153-03 A70-0308-05 A09-0078-08 | PANEL(TRAY) REMOCON ASSY(RC-P8020) BATTERY COVER | | |
| | 215 216 217 218 | 2E 2E 2E 2E 2E | * | B10-1047-04 B10-1048-03 B12-0066-04 B43-0287-04 B46-0092-03 | FRONT GLASS(REMOCON) FRONT GLASS(DISPLAY) INDICATOR KENWOOD BADGE WARRANTY CARD | К | |
| | - - - - | | * * | B46-0122-13 B46-0143-03 B50-9861-00 B50-9862-00 B50-9864-00 | WARRANTY CARD WARRANTY CARD INSTRUCTION MANUAL(ENGLISH) INSTRUCTION MANUAL(FRENCH) INSTRUCTION MANUAL(G,D,I) | E T E E | 00 00 |
| | 222 | 1 F | * | D21-1540-03 | EXTENSION SHAFT | | |
| | 225 226 227 228 228 | 1F 1E 1F 1G 1G | | E29-0333-04 E30-0505-05 E30-0977-05 E30-0459-05 E30-0780-05 | LEAD PLATE AUDIO CORD CORD WITH PLUG AC POWER CORD AC POWER CORD | K E K | ភភភភ |
| | 228 229 230 | 1G 2F 2F | | E30-1416-05 E31-4289-05 E31-4790-05 | AC POWER CORD WIRING HARNESS WIRING HARNESS | Т | s |
| | 235 | 1 G | | F11-0440-03 | SHIELDING CASE | | |
| | - | | * * | H01-8690-04 H10-3934-02 H10-3935-02 H25-0232-04 H25-0361-04 | ITEM CARTON CASE POLYSTYRENE FOAMED FIXTURE(L) POLYSTYRENE FOAMED FIXTURE(R) PROTECTION BAG (235X350X0.03) PROTECTION BAG | | |
| | 242 243 244 245 246 | 2F,2G 2G 2F 2F 1G,2G | | J02-1052-05 J11-0129-05 J19-2598-15 J19-0581-05 J19-0506-05 | FOOT ASSY WIRE CLAMPER UNIT HOLDER UNIT HOLDER(H=27.3) UNIT HOLDER(H= 8.3) | | |
| | 247 248 | 2G 2E | * | J19-3208-05 J21-3326-05 | UNIT HOLDER JACK MOUNTING HARDWARE | | |

E: Scandinavia & Europe K: USA

P: Canada

U: PX(Far East, Hawaii) T: England M: Other Areas UE : AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts

Parts without Parts No. are not supplied.

Les articles non mentionnes dans le Parts No. ne sont pas fournis.

Teile ohne Parts No. werden nicht geliefert.

| | Ref. No. | Address | New Parts | Parts No. | Description | Desti- nation | Re- marks |
|-----|---|----------------------------|--------------|--|--|------------------|--------------|
| | 参照番号 | 位置 | 新 | 部品番号 | 部 品 名 / 規 格 | | 備考 |
| Δ | 251 | 16 | * | J42-0083-05 J21-5560-04 J61-0307-05 | POWER CORD BUSHING MOUNTING HARDEARE WIRE BAND | KE | s |
| | 255 256 257 258 259 | 1F 2F 2F 2F 2E | * * | K27-2004-04 K29-3780-04 K29-3782-03 K29-3783-03 K29-3796-05 | KNOB (BUTTON)(POWER) KNOB (PLAY/PAUSE) KNOB (20KEY) KNOB (SKIP) KNOB ASSY(OUTPUT LEVEL) | | |
| | 262 262 | 1G 1G | * | L07-5601-05 L07-5602-05 | POWER TRANSFORMER POWER TRANSFORMER | K TE | S S |
| | A B C D E | | * | N89-3006-46 N89-3008-45 N89-4008-45 N09-2706-05 N09-2696-05 | BINDING HEAD TAPTITE SCREW BINDING HEAD TAPTITE SCREW BINDING HEAD TAPTITE SCREW TAPTITE SCREW STEPPED SCREW | | |
| - [| • | | | | IT (X25-3810-00) | 4 | |
| Ī | D1 -20 D21 | | | B30-1012-05 B30-1263-05 | LED(SLP-981C-50) LED | | |
| Δ | C1 C2 -5 | | | CE04KW1C330M CK45FF1H103Z | ELECTRO 33UF 16WV CERAMIC 0.010UF Z | | |
| | CN1 CN2 | | | E10-2703-05 E10-1908-05 | FLAT CABLE CONNECTOR FLAT CABLE CONNECTOR | | |
| | CP1 | | * | R90-0852-05 | MULTIPLE RESISTOR | | |
| | S1 -30 | | | S40-1064-05 | PUSH SWITCH | | |
| | D22 -32 D22 -32 D33 FL1 IC1 -3 | | * | HSS104A 1SS131 DAP803 FIP9BFM8 TD62801P | DIODE DIODE DIODE FLUORESCENT INDICATOR TUBE IC | | |
| | IC4 IC5 Q1 Q1 Q2 -4 | | * | UPD75216ACW-295 M51951ASL 2SC1740S(Q,R) 2SC945(A)(Q,P) DTA124EN | IC(MICROPROCESSOR) IC(SYSTEM RESET) TRANSISTOR TRANSISTOR DIGITAL TRANSISTOR | | |
| | Q5 Q5 Q6 | | | 2SC1740S(Q,R) 2SC945(A)(Q,P) 2SK105(F,H) | TRANSISTOR TRANSISTOR FET | | |
| | A1 | | | W02-0973-05 | ELECTRIC CIRCUIT MODULE | | |
| [| | OL UNIT | (X32 | ?-1510-XX) 11 : K, P 21 : | U, M, UE / JAPAN (X25-1572-71) X, / SIN | GAPORE | - |
| | C1 -4 C5 C6 C7 -9 C10 ,11 | | * | CF92FV1H103J CE04KW1C330M CF92FV1H221J CE04KW1C330M CE04KW1C331M | MF 0.010UF J ELECTRO 33UF 16WV MF 220PF J ELECTRO 33UF 16WV ELECTRO 330UF 16WV | | |
| | C12 ,13 C14 ,15 C16 ,17 C18 ,19 C20 ,21 | | * | CF92FV1H363J CF92FV1H821J CF92FV1H752J CF92FV1H103J CF92FV1H242J | MF 0.036UF J MF 820PF J MF 7500PF J MF 0.010UF J MF 2400PF J | | |
| | C22 ,23 | | | CF92FV1H561J | MF 560PF J | | |

E: Scandinavia & Europe K: USA

P: Canada

U: PX(Far East, Hawaii) T: England M: Other Areas

UE : AAFES(Europe) X: Australia

SINGAPORE MADE

PARTS LIST

Parts without Parts No. are not supplied.

Les articles non mentionnes dans le Parts No. ne sont pas fournis.

Telle ohne Parts No. werden nicht geliefent.

| Ref. | No. | Add | ress | New Parts | F | art | s N | о. | | | De | scription | | Desti- | Re- |
|--|-------------------------------------|-----|------|--------------|--------------------------------------|-------------------|-------------------------|--------------------|---|---|----|---|--|---------------|-------------|
| 参照 | 番号 | 位 | 懂 | Parts #π | 部 | 品 | 書 | 号 | | 部 | 品 | 名/規 | 格 | nation 仕 向 | marks 備考 |
| C28 C34 C36 | , 25 -33 , 35 , 37 , 39 | | | * | C90- CF92 CF92 CE04 CE04 | FV1 FV1 KW1 | H47 H22 A10 | 11J 11J 11M | ELECTRO MF MF ELECTRO ELECTRO | | | 22UF 470PF 220PF 100UF 220UF | 50WV J J 10WV 16WV | | |
| C42 C44 | , 41 , 43 , 45 , 47 | | | | CE04 CE04 CE04 CE04 | KWO KW1 KWO | J33 C33 J33 | 51M 50M 51M | ELECTRO ELECTRO ELECTRO ELECTRO ELECTRO | | | 1.0UF 330UF 33UF 330UF 100UF | 50WV 6.3WV 16WV 6.3WV 10WV | | |
| C50 C52 C54 C55 C56 | ,53 | | | | CE04 CE04 CC45 CK45 CK45 | KW1 FSL FB1 | A10 1H1 H33 | 01M .01J 32K | ELECTRO ELECTRO CERAMIC CERAMIC CERAMIC | | | 33UF 100UF 100PF 3300PF 0.010UF | 16WV 10WV J K Z | | |
| C58 C59 C61 C62 C63 | ,60 | | | | CF92 CK45 CC45 CC45 | FB1 FUJ FUJ | H22 1H3 1H1 | 2K 330J 01J | MF CERAMIC CERAMIC CERAMIC CERAMIC | | | 0.12UF 2200PF 33PF 100PF 5.0PF | C J K | | |
| C66 - | ,65 -68 ,70 ,72 | | | | CF92 CE04 CC45 CE04 CK45 | KW1 FSL KW1 | C33 1HC HO1 | 0M 040C 0M | MF ELECTRO CERAMIC ELECTRO CERAMIC | | | 1000PF 33UF 4.0PF 1.0UF 0.010UF | J 16WV C 50WV Z | | |
| C74 C75 C76 C77 C78 - | -80 | | | | CF92 CE04 CE04 CE04 | KW1 KW1 KW1 | C33 E33 H01 | OM OM | MF ELECTRO ELECTRO ELECTRO ELECTRO | | | 0.10UF 33UF 33UF 1.0UF 33UF | J 16WV 25WV 50WV 16WV | | |
| C81 C82 C84 C85 C86 | 83 | | | * | CK45 C90- C91- CF92 CF92 | 180 074 FV1 | 5-0 5-0 H10 | 15 15 12J | CERAMIC ELECTRO CERAMIC MF MF | | | 0.010UF 330UF 100PF 1000PF 270PF | Z 25WV K J J | | |
| C88 C90 C94 C95 C101, | . 89 -93 . 96 . 102 | | | | CF92 CF92 CK45 CE04 CE04 | FV1 FF1 KW1 | H27 H10 H01 | 2J 13Z .OM | MF MF CERAMIC ELECTRO ELECTRO | | | 2200PF 2700PF 0.010UF 1.0UF 33UF | J J Z 50WV 16WV | | |
| C103 C104 C105 C106 C107 | | | | | CK45 CE04 CE04 CF92 CF92 | KW1 KW1 FV1 | HR4 A10 H10 | .7M 11M 13J | CERAMIC ELECTRO ELECTRO MF MF | | | 0.010UF 0.47UF 100UF 0.010UF 1000PF | Z 50WV 10WV J J | | |
| C108- C113 C114 C115 C117, | | | | | CE04 CK45 CK45 CE04 CK45 | FSL FF1 KW1 | 1H1 H1C C33 | 80J 32 0M | ELECTRO CERAMIC CERAMIC ELECTRO CERAMIC | | | 33UF 18PF 0.010UF 33UF 0.010UF | 16WV J Z 16WV Z | | |
| C119 C120, C122 C123 C124, | | | | | CE04 CC45 CF92 C90- CE04 | FSL FV1 134 | 1 H 1 H 3 3 9 - 0 | .50J !3J !5 | ELECTRO CERAMIC MF NP-ELEC ELECTRO | | | 33UF 15PF 0.033UF 1UF 33UF | 16WV J J 50WV 16WV | | |

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* New Parts

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| 1 | 磐 照 | 書 | 号 | 位 | 鷕 | 新 | 部 | 品 | 番 号 | | 部 | 品 | 名/ | 規 | 格 | | 備考 |
| CCC | 126 127 128 129 131 | | | | | | C90-1 CF92F CF92F CF92F C91-0 | V1F V1F V1F | 1223J 1152J 1222J | | NP-ELEC MF MF MF CERAMIC | | 2.2U 0.02 1500 2200 0.00 | 2UF PF PF | 50WV J J J F K | | |
| 000 | 132 133 136 137 139 | , 1 , 1 | | | | | | FII FII | 1822J | J | CERAMIC CERAMIC CERAMIC MF NP-ELEC | | 0.01 100P 0.01 8200 0.47 | F OUF PF | Z J Z J 50WV | | |
| 000 | 140 141 142 143 145 | , 1 | 44 | | | | CE041 C90-1 CE041 | (W1/ L349 (W1(| 1H470. A101M 9-05 C330M H124J | Ţ | CERAMIC ELECTRO NP-ELEC ELECTRO MF | | 47PF 100U 1UF 33UF 0.12 | F | J 10WV 50WV 16WV J | | |
| 000 | 146 147 148 149 | | | | | | CK45 | 35 V11 B11 | | | NP-ELEC NP-ELEC MF CERAMIC MF | | 1UF 3.3U 0.10 820P 1000 | UF F | 50WV 50WV J K J | | |
| 000 | 151 152 153 155 157 | | | | | | CF 925 CK 455 C91-0 | F11 7F11 | 1H121. H104J H103Z 8-05 V100M | J | CERAMIC MF CERAMIC CERAMIC ELECTRO | | 120P 0.10 0.01 0.00 10UF | UF OUF 147U | J J Z F K 35WV | | |
| 000 | 160 161 163 164 205 | , 1 | | | | | C90-1 C90-1 C91-0 CE041 C90-1 | 134° 065: (W1) | 9-05 2-05 E330M | | NP-ELEC CERAMIC ELECTRO NP-ELEC | | 2.2U 1UF 0.00 33UF 0.1U | 1UF | 50WV 50WV K 25WV 50WV | | |
| 000 | 207 209 213 215 301 | -2 ,2 | 12 14 | | | | C90- | (W1) 145 (W1) | C330M 6-05 H010M | | NP-ELEC ELECTRO NP-ELEC ELECTRO FILM | | 1UF 33UF 0.22 1.0U 0.01 | UF IF | 50WV 16WV 50WV 50WV 250WV | | |
| 000 | 304 306 308 312 313 | , 3 -3 | 07 | | | | CEO41 CF921 CEO41 | (W1) (W1) (W1) | H103J E102M H103J C222M H470M | | MF ELECTRO MF ELECTRO ELECTRO | | 0.01 1000 0.01 2200 47UF | UF OUF OUF | J 25WV J 16WV 50WV | | |
| | 314 318 | | 15 | | | | | | A222M H105J | | ELECTRO MF | | 2200 1.00 | | 10WV J | | |
| C J J | N1 N2 301 302 303 | | | The state of the s | | * | E10-: E10- E13- E11-: E11-: | 190 140 018 | 7-05 4-05 8-05 | | FLAT CABLI FLAT CABLI PHONO JACI MINIATURE PHONE JACI | C (4) (4) PH | DNNEC P) LI DNE J | TOR NE IACK | OUT (System) | | |
| - | | | | | | | F01- | 046 | 8-04 | | HEAT SINK | | | | | | |
| - | | | | | | * | J21- | 551 | 6-04 | | MOUNTING | HAR | DWARE | 3 | | | |
| L | .1 .4 .5 | -3 -8 | | | | | L40- L32- L40- L40- | 032 101 | 8-15 1-17 | | SMALL FIXI OSCILATING SMALL FIXI SMALL FIXI | G CI Ed | SIL Induc | TOR | (100UH,K) | | |

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| Ref. No. 参照書号 | Address 位 置 | New Parts 新 | Parts No. 部品番号 | Description 部 品 名 / 規 格 | | Re- mark 備考 |
|---|----------------|-------------------|--|---|------|-------------------|
| L11 ,12 L101 L311 X1 | | | L40-1011-17 L40-1001-17 L79-0733-05 L77-1164-05 | SMALL FIXED INDUCTOR(100UH,K) SMALL FIXED INDUCTOR(10UH,K) LINE FILTER CRYSTAL RESONATOR | | |
| F G | | | N30-3006-46 N89-3008-46 | PAN HEAD MACHINE SCREW BINDING HEAD TAPTITE SCREW | | |
| R8 ,9 R13 ,14 R15 -18 R19 ,20 R21 ,22 | | | RD14AB2E220J . RN14BK2C4220F RN14BK2C1D01F RN14BK2C2371F RN14BK2C1001F | FL-PROOF RD 22 | | |
| R29 -32 R33 ,34 R35 ,36 R39 ,40 R41 -44 | | | RN14BK2C1001F RN14BK2C1003F RN14BK2C10R0F R92-0393-05 RN14BK2C1963F | RN 1.00K F 1/6W RN 100K F 1/6W RN 10.0 F 1/6W RD 3.0K J 1/2W RN 196K F 1/6W | | |
| R70 R75 R92 VR1 -4 VR101-103 | | * | RN14BK2C1004F RS14KB3A560J RS14KB3A101J R12-5070-05 R12-3126-05 | RN 1.00M F 1/6W FL-PROOF RS 56 J 1W FL-PROOF RS 100 J 1W TRIMMING POT.(2SB,MSB) TRIMMING POT.(7F GAIN&BIAS) | | |
| VR104 VR201 | | * | R12-3128-05 R29-9023-05 | TRIMMING POT. (TE BALANCE) POTENTIOMETER (3KX2) OUTPUT | | |
| K1 S1 S2 | | | S51-2089-05 S40-1103-05 S31-2131-05 | MAGNETIC RELAY PUSH SWITCH (POWER TYPE) SLIDE SWITCH (POWER TYPE) | UMUE | |
| D1 ,2 D1 ,2 D3 ,4 D3 ,4 D5 ,6 | | | HZS8.2N(B) RD8.2ES(B) HZS4.7N(B) RD4.7ES(B) HZS13N(B2) | ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE | | |
| D5 ,6 D7 D7 D8 D8 | | | RD13ES(B2) HZS5.6N(B2) RD5.6ES(B2) HSS104 1SS133 | ZENER DIODE ZENER DIODE ZENER DIODE DIODE DIODE | | |
| D9 D10 ,11 D10 ,11 D12 ,13 D12 ,13 | | | 1SV147 HZS11N(B2) RD11ES(B2) HZS5.1N(B2) RD5.1ES(B2) | VARISTOR ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE | | |
| D14 ,15 D14 ,15 D16 -19 D16 -19 D105 | , , | | HZS5.6N(B2) RD5.6ES(B2) HSS104 1SS133 HSS104 | ZENER DIODE ZENER DIODE DIODE DIODE DIODE DIODE | | |
| D105 D106 D106 D107 D107 | | | 1SS133 HZS5.6N(B2) RD5.6ES(B2) HSS104 1SS133 | DIODE ZENER DIODE ZENER DIODE DIODE DIODE | | |
| D108 D108 | | | HZS30N(B) RD30ES(B) | ZENER DIODE ZENER DIODE | | |

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♠ indicates safety critical components.

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| D109 D109 D110-112 D110-112 D115-117 | | | HZS7.5S(B) RD7.5JS(B) HZS4.7N(B) RD4.7ES(B) HSS104 | ZENER DIODE ZENER DIODE ZENER DIODE ZENER DIODE DIODE | |
| D115-117 D120,121 D120,121 D201-204 D201-204 | | | 1SS133 HSS104 1SS133 HSS104 1SS133 | DIODE DIODE DIODE DIODE | |
| D301-304 D305 D305 D306-311 IC1 -3 | | | S5566B HSS104A 1SS131 S5566B NJM4565D | DIODE DIODE DIODE DIODE IC(OP AMP X2) | |
| IC4 ,5 IC6 ,7 IC8 IC9 IC10 | : | * | NJM4580D PCM1701P NJM4565D SM5813AP TC74HCU04AP | IC IC IC(OP AMP X2) IC(OPS DIGITAL FILTER) IC(CMOS INVERTER) | |
| IC11 IC12 IC13 IC14 IC15 | | | CXD1165Q NJM4565D KAG01 NJM4565D TC74HC00AP | IC(DIGITAL SIGNAL PROCESSOR) IC(OP AMP X2) CUSTOM IC IC(OP AMP X2) IC(QUAD 2-INPUT NAND GATE) | |
| IC101 IC102 IC103 IC104 IC105 | | | NJM4558D UPD4053BC CXA1244S CXA1081S NJM4558D | IC(0P AMP X2) IC(3-INPUT 2CH MPX/DE-MPX) IC(SERVO SIGNAL PROCESSOR) IC(RF AMP) IC(0P AMP X2) | |
| IC106 IC109,110 IC201 Q1 Q2 | | | TC74HC00AP NJM4558D NJM4565D 2SB941 2SD1266 | IC(QUAD 2-INPUT NAND GATE) IC(OP AMP X2) IC(OP AMP X2) TRANSISTOR TRANSISTOR | |
| Q3 Q4 Q4 Q5 ,6 Q7 ,8 | | | DTC124EN 2SC1740S(Q,R) 2SC945(A)(Q,P) 2SC2878(B) 2SA1206 | DIGITAL TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR | |
| Q9 ,10 Q11 ,12 Q13 -16 Q17 Q18 | | | 2SK246 2SK152 2SC3940A 2SA1534A 2SC3940A | FET FET TRANSISTOR TRANSISTOR TRANSISTOR | |
| 919 920 ,21 920 ,21 922 9101 | | | 2SK246 2SA733(A)(Q,P) 2SA933S(Q,R) DTA124EN 2SA1534A | FET TRANSISTOR TRANSISTOR OIGITAL TRANSISTOR TRANSISTOR | |
| 9102 9103 9104,105 9106 9107 | | | 2SC3940A 2SD1944 2SA1534A 2SC3940A 2SA1534A | TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR | |

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UE : AAFES(Europe) X: Australia

U: PX(Far East, Hawaii) T: England M: Other Areas

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PARTS LIST

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| 9108 9109 9110 9111 9112 | | | 2SC3940A 2SA1534A 2SC3940A 2SA1534A 2SC3940A | TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR | | |
| 9113 9114 9115 9116 9118 | | | 2SA1534A 2SC3940A 2SA1534A 2SC3940A 2SA1534A | TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR TRANSISTOR | | |
| Q201,202 Q203,204 | | | 2SC3666 2SA1426 | TRANSISTOR TRANSISTOR | | |
| A 1 | | | W02-1036-05 | TRANSMITTING ASSY(OPT OUT) | | |
| | | M | ECHANISM ASS'Y | (X92-1370-02) / JAPAN | | |
| 1 2 3 4 | 1 A 2 A 3 B 2 B | * | A10-1964-01 A11-0626-15 A11-0621-08 A11-0623-08 | CHASSIS SUB CHASSIS ASSY SUB CHASSIS INJECTION MOLD SUB CHASSIS | | |
| 8 | 2B | | B09-0098-08 | CAP | | |
| 13 13 14 15 16 | 3B 3B 1B 3B 1B | | D02-0091-08 D02-0092-08 D10-2324-03 D10-2325-04 D13-0807-04 | TURNTABLE PLATTER TURNTABLE PLATTER SLIDER RØD GEAR | | |
| 17 18 19 20 21 | 1B 3B 3B 3B 3B 1B | | D13-0808-02 D13-0809-08 D13-0810-04 D13-0811-04 D13-0813-04 | GEAR GEAR GEAR GEAR GEAR | | |
| 22 23 | 2B 1B | | D15-0296-04 D16-0282-04 | MOTOR PULLEY BELT | | |
| 27 28 29 30 | 1B 2B 2B 2B | * | E23-0343-04 E31-7270-05 E31-7271-05 E31-7075-05 | TERMINAL WIRING HARNESS (WHITE/BLUE) WIRING HARNESS (WHITE/RED) WIRING HARNESS | | |
| 35 | 1 B | | F19-1005-04 | BLIND PLATE | | |
| 38 39 40 41 42 | 2B 2B 1B 1B 2A | | G01-2385-08 G01-2390-08 G02-0926-04 G02-0927-04 G16-0739-04 | COMPRESSION SPRING COMPRESSION SPRING FLAT SPRING FLAT SPRING SHEET | | |
| 43 44 45 | 2A 1B 1B | * | G16-0744-04 G02-0945-04 G11-2008-04 | SHEET FLAT SPRING ASSY CUSHION | | |
| 47 48 49 51 52 | 2B 2B 2B 2A 2A | | J02-1033-08 J11-0151-03 J91-0385-08 J99-0065-11 J99-0067-13 | INSULATOR CLAMPER PICKUP TRAY TRAY ASSY | | |
| A B | | | N35-2605-46 N09-1522-05 | BINDING HEAD MACHINE SCREW SET SCREW (3X8) | | |
| | Ĺ | | | † | 1 1 | |

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| 参照番号 | 位置 | Parts 新 | 部品番号 | 部品名/規格 任 | | marks 備考 |
| C D E F G | | | N39-2025-46 N09-2705-05 N89-2610-46 N19-1179-05 N89-2608-46 | PAN HEAD MACHINE SCREW MACHINE SCREW BINDING HEAD TAPTITE SCREW FLAT WASHER BINDING HEAD TAPTITE SCREW | | |
| н | | | N88-3008-45 | FLAT HEAD TAPTITE SCREW | | |
| 55 56 | 38 28 | | S33-1022-05 S33-2061-05 | LEVER SWITCH LEVER SWITCH | | |
| 60 61 62 63 64 | 2B 3B 3B 2B 2B 2B | | T42-0530-05 T42-0531-05 T42-0532-05 T50-1044-04 T99-0233-05 | DC MOTOR DC MOTOR DC MOTOR YOKE MAGNET | | |
| | | ME | CHANISM ASS'Y (| X92-1400-02) / SINGAPORE | | |
| 101 104 | 1C 3D | | A10-2513-01 A11-0625-02 | CHASSIS SUB CHASSIS | | S S |
| 114 115 116 117 | 1D 2D 1D 1D | | D10-2324-03 D10-2315-04 D13-0807-04 D13-0808-02 | SLIDER RØD GEAR(INTERMEDIATE) GEAR(MAIN) | | s |
| 119 | 2D | | D13-0802-08 | GEAR(A) | | S |
| 120 121 122 123 124 | 2D 1D 2D 1D 2D | | D13-0803-08 D13-0813-04 D15-0296-04 D16-0284-03 D40-0876-05 | GEAR(B) GEAR(PULLEY) MOTOR PULLEY BELT MECHANISH ASSY | | S |
| 125 126 127 | 1D 1D 1D | * | G11-2008-04 G02-0945-04 E23-0343-04 | CUSHION FLAT SPRING ASSY TERMINAL(SHORT) | | |
| 128 129 130 131 | 2D 2D 2D 3D | * | E31-7236-15 E31-7237-05 E31-7137-05 E40-4117-08 | WIRING HARNESS(WHITE/BLUE) WIRING HARNESS(WHITE/RED) WIRING HARNESS(5P) CONNECTOR PIN(4P) | | 2000 |
| 134 135 | 2D 1D | | F07-0554-08 F19-1015-14 | GEAR COVER BLIND PLATE | | s |
| 138 139 140 141 142 | 3D 3D 1D 1D 2C | | G01-2394-04 G01-2395-04 G02-0926-04 G02-0927-04 G16-0743-04 | COMPRESSION SPRING(FRONT) COMPRESSION SPRING(REAR) FLAT SPRING(L) FLAT SPRING(R) SHEET | | 55 |
| 143 | 2C | | G16-0745-04 | SHEET | | S |
| 144 | 2D | | J19-3148-08 | SHAFT CLAMP | | s |
| 145 146 147 148 | 3D 2D 3D 2D | | J25-6135-08 J90-0640-08 J02-1027-08 J11-0130-03 | MOTOR PCB SLIDER HOLDER(J) INSULATOR CLAMPER | | S S S |
| 149 150 151 152 | 2D 3D 1C 2C | * | J91-0385-08 J42-0175-04 J99-0069-11 J99-0070-13 | PICKUP(KSS-150A(H)) BUSHIHG TRAY TRAY ASSY | | 555 |
| A | | | N35-2605-46 | BINDING HEAD MACHINE SCREW | | |

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| | 71 | N09-1522-05 N39-2005-46 N89-2608-46 N09-2670-08 N09-2671-08 | SET SCREW (3X8) PAN HEAD MACHINE SCREW BINDING HEAD TAPTITE SCREW SCREW SCREW | 17 141 | S |
| | | N89-2606-46 N19-1217-04 | BIND HEAD TAPTITE SCREW FLAT WASHER | | s |
| 3D 2D | | S46-1128-08 S33-2061-05 | LEAF SWITCH(S1/LIMIT) LEVER SWITCH(S2/OPEN,CLOSE) | | s |
| 2D 2D 3D 2D 2D | | T42-0530-05 T42-0528-08 T42-0527-08 T50-1046-04 T99-0233-05 | DC MOTOR(M3/TRAY) DC MOTOR(M2/SPINDLE) DC MOTOR(M1/FEE) YOKE MAGNET | | S |
| | | | | | |
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U: PX(Far East, Hawaii) T: England M: Other Areas UE : AAFES(Europe) X: Australia

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DP-7020 DP-7020

SPECIFICATIONS

| [Format] | Output | | | |
|--|----------------------------------|--|--|--|
| Type Compact disc player | LINE (FIXED) | | | |
| Read system Non-contact optical pick-up | DIGITAL (OPTICAL)15 dBm ~ -21 dB | | | |
| Rotational speed About 200 rpm to 500 rpm | Headphone jack 20 mW (8 Ω) | | | |
| [Audio] | [General] | | | |
| Frequency response 2 Hz ~ 20 kHz ±0.5 dB | Power consumption | | | |
| Signal-to-noise ratio more than 110 db | Dimensions | | | |
| Total narmonic distortion 0.0025% at 1 kHz | H: 128 mm (5-1/16") | | | |
| Channel separation more than 105 dB at 1 kHz | D: 314 mm (12-3/8") | | | |
| Wow & flutter Below measurable limit | Weight 5.9 kg (13.0 lb) | | | |

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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200 Esat Dominguez Street, Long Beach. CA 90810:
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